# What you always wanted to know about Colpitts Oscillators

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**Introduction:** Modern communications systems need oscillators as part of the design. In most cases these oscillators are part of a synthesizer and they are voltage controlled, meaning that the frequency is determined by tuning diodes, frequently called varactors. The applied DC voltage varies the frequency. For high performance circuits the Colpitts Oscillator is most frequently selected [1-30].

The Colpitts oscillator comes in three flavors – Figure 1a, shows the conventional circuit configuration. This type of circuit is based on a design developed by Edwin Henry Colpitts known for his invention of this oscillator and hence carries his name [1]. It uses a capacitive voltage divider and an inductor. In reality this simple circuit is not used but rather a derivation of this. This is shown in Figure 1b. The advantage of this circuit is that the values for $C_1$ and $C_2$ are fixed and the frequency change occurs by changing $C_3$. If the frequency of Figure 1a needs to be changed, a better choice is to vary the inductor L.

His colleague Ralph Hartley [2] invented an inductive coupling oscillator. The advantage of such an oscillator having capacitors $C_1$ and $C_2$ replaced with a tap of the inductor has been used together with helical resonators. The frequency tuning is achieved purely capacitively. To minimize loading, the transistor of choice here is a FET which has very high input impedance and provides minimum loading to the circuit. The disadvantage is that this circuit, using junction FETs, is limited to about 400 MHz. The transition frequency $f_T$ is about 500MHz. FETs can also be used in the Colpitts oscillator as shown in Figure 1a, because of relatively lower loading than the bipolar transistor. The drawback of Figure 1a

is the heavy loading of the tuned circuit by the transistor. The circuit shown in Figure 1b is frequently referred to as the Clapp-Gouriet circuit [3].

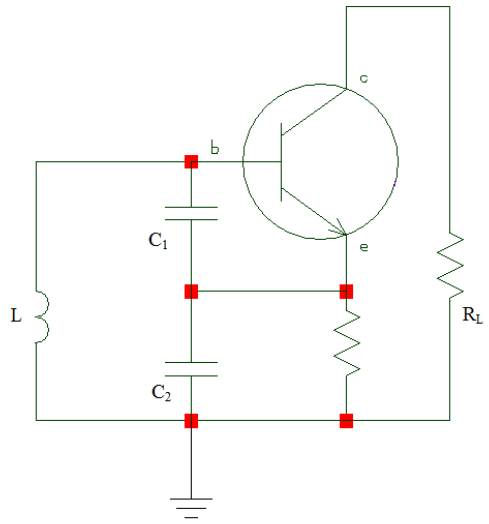


**Figure 1a: Conventional Colpitts Configuration**

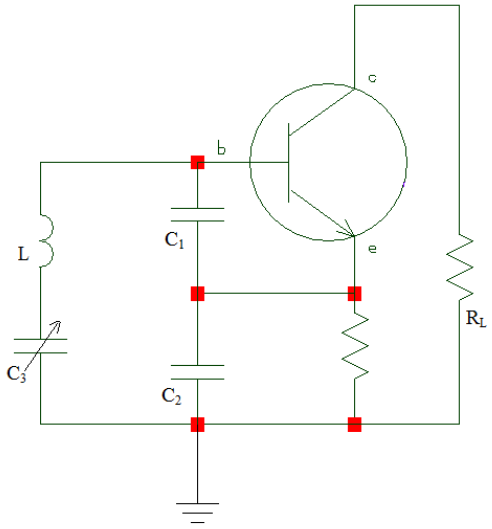


**Figure1b: Modified Colpitts (Clapp-Gouriet) Config.**

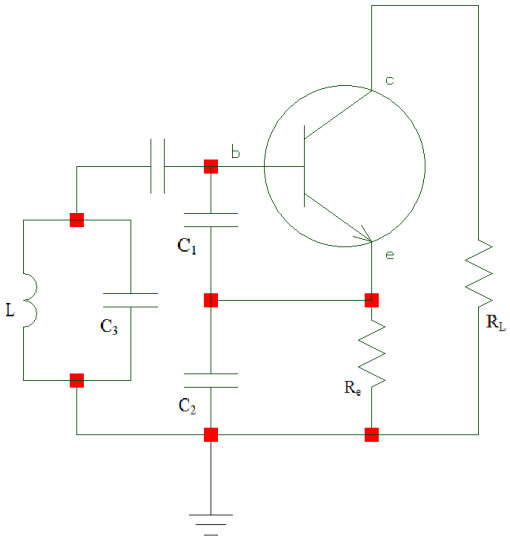


**Figure 1c: Modified Colpitts Oscillator**

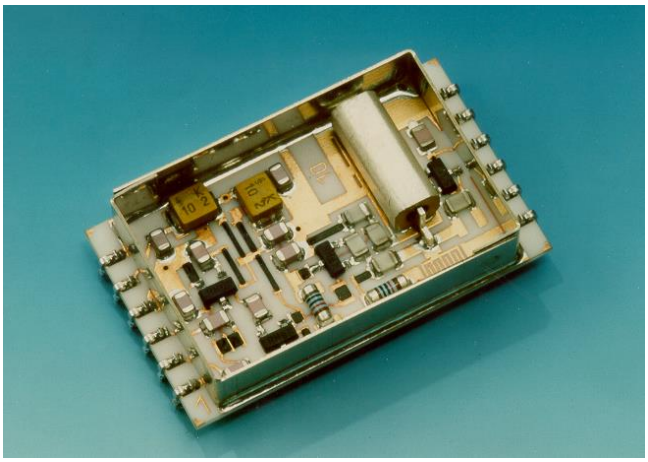

**Figure 2: Photograph of 1 GHz CRO**

At frequencies below 1GHz, both GaAs FETs and CMOS FETs are not a good choice because of their high flicker noise contribution.

For the circuit of Figure 1b, it is theoretically possible to have L and $C_3$ in resonance in which case the oscillator will cease to work. It is important to note here that the same circuit is used also for crystal oscillators; here the inductor L is replaced by the crystal. The crystal is a series combination of $L_s$, $R_s$ and $C_s$ with $Q = \omega L/R$. In practice the product of crystal Q and frequency is a constant. For 5 MHz, a typical Q of $2.5\times10^6$ is possible, resulting in a product of $12.5\times10^{12}$. If this is scaled to a crystal oscillator operating at 100MHz, the Q would be 125000. Manufacturers typically guarantee values greater than 100000.

Again, this crystal oscillator also falls into the category of Colpitts oscillator. A third variation is shown in Figure 1c. Here we have a parallel tuned circuit which is coupled loosely to the transistor. This circuit is found when building oscillators using ceramic resonators (CRO). Figure 2 shows such a design.

This paper summarizes the various methods of oscillator analysis and presents a step-by-step design procedure, showing the simulated, measured and calculated results for phase noise and other important parameters and concludes with a discussion on the effect of tuning diodes.

**Linear Approach:** For many years, until recently, oscillators were analyzed with a linear approach as will be shown below. Figures 3a and 3b illustrate the oscillator sub-circuit for the purpose of calculating the negative resistance.

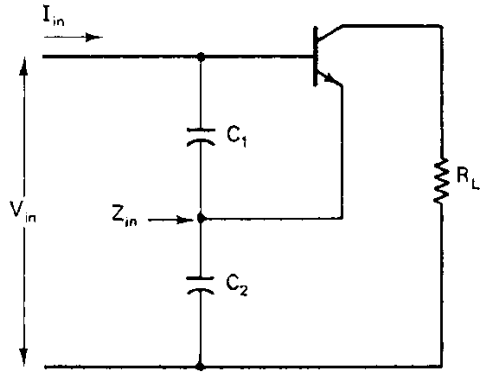


**Figure 3a: Oscillator sub-circuit for impedance analysis**

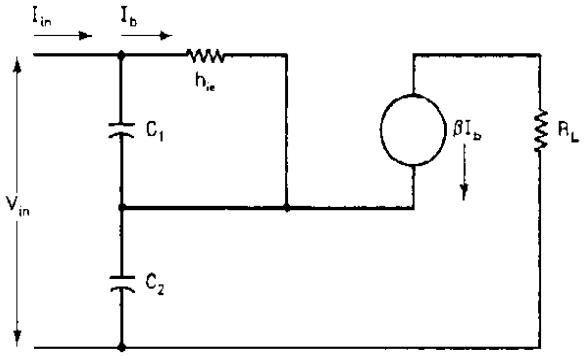


**Figure 3b: Equivalent sub-oscillator circuit for the calculation of the negative resistance**

From Figure 3b, the circuit equation is given from Kirchoff's voltage law (KVL) as

$$V_{\text{in}} = I_{\text{in}}\left(X_{C_1} + X_{C_2}\right) - I_b\left(X_{C_1} - \beta X_{C_2}\right) \tag{1a}$$

$$0 = -I_{\text{in}}\left(X_{C_1}\right) + I_b\left(X_{C_1} + h_{ie}\right) \tag{1b}$$

Considering, $\dfrac{1}{Y_{11}} = h_{ie}$

$$Z_{\text{in}} = \frac{V_{\text{in}}}{I_{\text{in}}} = \frac{(1+\beta)X_{C_1}X_{C_2} + h_{ie}\left(X_{C_1} + X_{C_2}\right)}{X_{C_1} + h_{ie}} \tag{1c}$$

$$Z_{\text{in}} = \frac{\left(-\dfrac{(1+\beta)}{\omega^2 C_1 C_2} + \dfrac{(C_1 + C_2)}{j\omega C_1 C_2}\dfrac{1}{Y_{11}}\right)}{\left(\dfrac{1}{Y_{11}} + \dfrac{1}{j\omega C_1}\right)} \tag{1d}$$

The input impedance ($Z_{IN}$) of this Colpitts Oscillator circuit, including the parasitics is given as [4, 5]:

$$Z_{IN}\big|_{pacakage} = -\left[\frac{Y_{21}}{\omega^2(C_1 + C_p)C_2}\frac{1}{(1+\omega^2 Y_{21}^2 L_p^2)}\right] - j\left[\frac{(C_1 + C_P + C_2)}{\omega(C_1 + C_P)C_2} - \frac{\omega Y_{21} L_P}{(1+\omega^2 Y_{21}^2 L_p^2)}\frac{Y_{21}}{\omega(C_1 + C_P)C_2}\right] \tag{2}$$

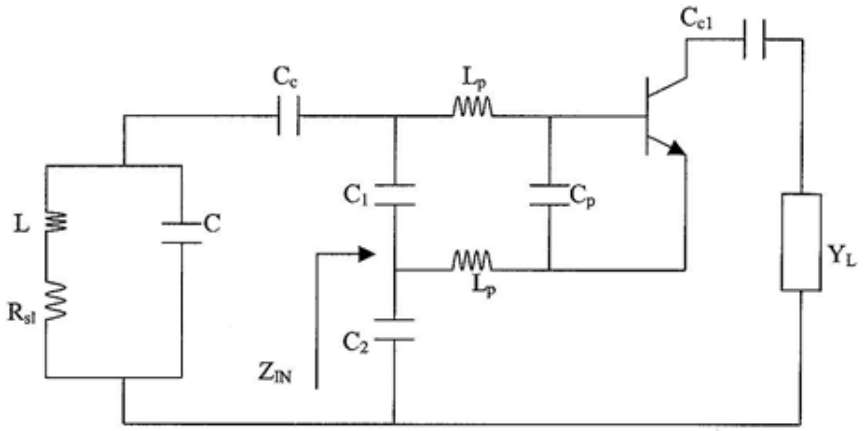


**Figure 3c: Colpitts oscillator with base lead inductances and package capacitance**

The resonator losses are expressed by the $R_{s1}$. Now splitting the $Z_{IN}$ of the Colpitts oscillator into real and imaginary parts, including parasitics, we obtain,

$$R_{NEQ} = \frac{R_N}{(1+\omega^2 Y_{21}^2 L_p^2)} \tag{3}$$

$$\frac{1}{C_{EQ}} = \left\{ \left[ \frac{1}{\frac{(C_1+C_P)C_2}{(C_1+C_2+C_P)}} \right] - \left[ \frac{\omega^2 Y_{21} L_P}{(1+\omega^2 Y_{21}^2 L_P^2)} \right] \left[ \frac{Y_{21}}{\omega(C_1+C_P)C_2} \right] \right\} \tag{4}$$

$$R_N = -\frac{Y_{21}}{\omega^2 C_1 C_2} \tag{5}$$

where

$R_N$ : Negative resistance without lead inductance and package capacitance.

$R_{NEQ}$ : Negative resistance with base-lead inductance and package capacitance.

$C_{EQ}$ : Equivalent capacitance with base-lead inductance and package capacitance

The method shown above is called one-port oscillator design [6]. Figure 4 shows the general schematic diagram of a one-port negative-resistance model. The negative real part of $Z_{IN}$ is used to compensate the losses of the parallel tuned circuit.

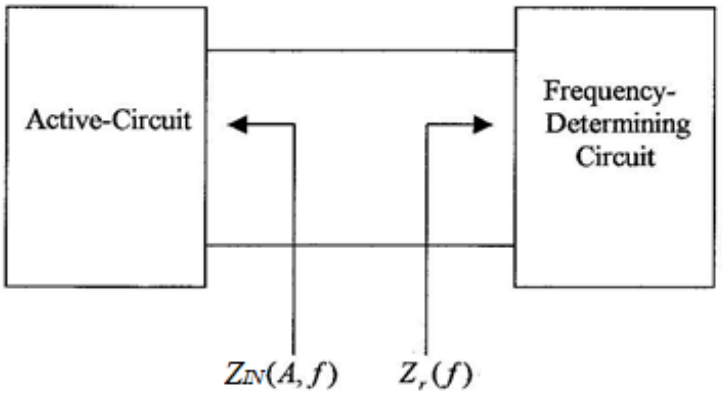


**Figure 4: Schematic diagram of a one-port negative resistance model**

**Linear S-parameters approach:**

It may be interesting for the readers to see how an oscillator can be analyzed using S-parameters. It should be noted that this method is based on linear approximations and works for practically all microwave oscillator designs [6, 28, pp-741]. The equivalent criteria of the negative resistance can be calculated in the form of S-parameters. The detailed definitions of S-parameters can be found in [31]. This negative resistance will cause oscillations if the following conditions are satisfied. Assume that the oscillation condition is satisfied at port 1 and is given by:

$$\frac{1}{S'_{11}} = \Gamma_G \tag{6}$$

Thus,
$$S'_{11} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1-S_{22}\Gamma_L} = \frac{S_{11}-D\Gamma_L}{1-S_{22}\Gamma_L} \tag{7}$$

$$\frac{1}{S'_{11}} = \frac{1-S_{22}\Gamma_L}{S_{11}-D\Gamma_L} = \Gamma_G \tag{8}$$

From expanding (7) we get

$$\Gamma_G S_{11} - D\Gamma_L\Gamma_G = 1 - S_{22}\Gamma_L \tag{9}$$

$$\Gamma_L(S_{22} - D\Gamma_G) = 1 - S_{11}\Gamma_G \tag{10}$$

$$\Gamma_L = \frac{1-S_{11}\Gamma_G}{S_{22}-D\Gamma_G} \tag{11}$$

$$S'_{22} = S_{22} + \frac{S_{12}S_{21}\Gamma_G}{1-S_{11}\Gamma_G} = \frac{S_{22}-D\Gamma_G}{1-S_{11}\Gamma_G} \tag{12}$$

$$\frac{1}{S'_{22}} = \frac{1-S_{11}\Gamma_G}{S_{22}-D\Gamma_G} \tag{13}$$

Comparing equations (9) and (12), we find that

$$\frac{1}{S'_{22}} = \Gamma_G \tag{14}$$

where, $S_{11}$ and $S_{22}$ are the input and output reflection coefficients, respectively

The discussion above means that the oscillation condition is also satisfied at port 2; which proves the simultaneous oscillation condition at both ports. Thus if either port is oscillating the other port must be oscillating as well. A load may appear at either or both ports, but normally the load is in $\Gamma_L$, the output termintation.

It is helpful to use the common-source based amplifier to compute the oscillator output power. For oscillators, the objective is to maximize ($P_{out} - P_{in}$) of the amplifier, which is the useful power to the load. An empirical expression for the common-source amplifier output power found by Johnson [29] is

$$P_{out} = P_{sat}\left(1 - exp\frac{-GP_{in}}{P_{sat}}\right) \tag{15}$$

Where $P_{sat}$ is the saturated output power of the amplifier and G is the tuned small-signal common-source transducer gain of the amplifier, which is identical to $|S_{21}|^2$. Since the objective is to maximize ($P_{out}$ - $P_{in}$), (where $P_{out}$ and $P_{in}$ are the output and input power of the amplifier),

$$d(P_{out} - P_{in}) = 0 \tag{16}$$

$$\frac{\partial P_{out}}{\partial P_{in}} = 1 \tag{17}$$

$$\frac{\partial P_{out}}{\partial P_{in}} = G_{exp} - \frac{GP_{in}}{P_{sat}} = 1 \quad (18)$$

$$exp\frac{GP_{in}}{P_{sat}} = G \quad (19)$$

$$\frac{P_{in}}{P_{sat}} = \frac{\ln G}{G} \quad (20)$$

At the maximum value of $(P_{out} - P_{in})$, the amplifier output is

$$P_{out} = P_{sat}(1 - \frac{1}{G}) \quad (21)$$

And the maximum oscillator output power is

$$P_{osc} = (P_{out} - P_{in}) \quad (22)$$

$$= P_{sat}\left(1 - \frac{1}{G} - \frac{\ln G}{G}\right) \quad (23)$$

Thus the maximum oscillator output power can be predicted from the common-source amplifier saturated output power and the small signal common source transducer gain G. For high oscillator output power high (loop) gain is of importance. Another definition of gain that is useful for large-signal amplifier or oscillator design is the maximum efficient gain, defined by

$$G_{ME} = \frac{P_{out} - P_{in}}{P_{in}} \quad (24)$$

For maximum oscillator power the maximum efficient gain from (20) and (21) is

$$G_{MEmax} = \frac{G-1}{lnG} \quad (25)$$

The RF gain $G_{MEmax}$ is a considerably smaller value compared to G, the small-signal gain [7-12].

Designing oscillators based on S-parameters in a linear mode has been quoted by many authors using first approximation for large signal as shown in [8]. The problem with this published approach is that it uses a GaAs FET, where only the transconductance $g_m$ has a major influence. $S_{11}$ changes very little under large signal conditions, as does $S_{22}$. Reliable large signal S-parameters for bipolar transistors and FETs are difficult to get.

**Time-domain based analysis to analyze the transistor non-linarities':**

A correction for the frequency dependent parameters will follow, based on "simulation" for larger drive level.

The voltage $v(t)$ across the base-emitter junction consists of a DC component and a driven signal voltage $V_1 \cos(wt)$. It can be expressed as

$$v(t) = V_{dc} + V_1 \cos(wt) \tag{26}$$

As the driven voltage $V_1 \cos(wt)$ increases and develops enough amplitude across the base-emitter junction, the resulting current is a periodic series of pulses whose amplitude depends on the nonlinear characteristics of the device and is given as

$$i_e(t) = I_s e^{\frac{qv(t)}{kT}} \tag{27}$$

$$i_e(t) = I_s e^{\frac{qV_{dc}}{kT}} e^{\frac{qV_1 \cos(wt)}{kT}} \tag{28}$$

$$i_e(t) = I_s e^{\frac{qV_{dc}}{kT}} e^{x\cos(wt)} \tag{29}$$

assuming $I_c \approx I_e$ ($\beta$>10)

$$x = \frac{V_1}{(kT/q)} = \frac{qV_1}{kT} \tag{30}$$

$i_e(t)$ is the emitter current and $x$ is the drive level which is normalized to $kT/q$.

From the Fourier series expansion, $e^{x\cos(wt)}$ is expressed as

$$e^{x\cos(wt)} = \sum_n a_n(x)\cos(nwt) \tag{31}$$

$a_n(x)$ is a Fourier coefficient and given as

$$a_0(x)\big|_{n=0} = \frac{1}{2\pi}\int_0^{2\pi} e^{x\cos(wt)}d(wt) = I_0(x) \tag{32}$$

$$a_n(x)\big|_{n>0} = \frac{1}{2\pi}\int_0^{2\pi} e^{x\cos(wt)}\cos(nwt)d(wt) = I_n(x) \tag{33}$$

$$e^{x\cos(wt)} = \sum_n a_n(x)\cos(nwt) = I_0(x) + 2\sum_1^{\infty} I_n(x)\cos(nwt) \tag{34}$$

$I_n(x)$ is the modified Bessel function.

$$\text{As } x \to 0 \Rightarrow I_n(x) \to \frac{(x/2)^n}{n!} \tag{35}$$

$I_0(x)$ are monotonic functions having positive values for x≥0 and n≥0; $I_0(0)$ is unity, whereas all higher order functions start at zero.

The short current pulses are generated from the growing large-signal drive level across the base-emitter junction, which leads to strong harmonic generation [5, 27]. The advantage of this pulse performance is the reduction of phase noise, due to the smaller duty cycle of the transistor [4]. The emitter current represented above can be expressed in terms of harmonics as

$$i_e(t) = I_s e^{\frac{qV_{dc}}{kT}} I_0(x)\left[1 + 2\sum_1^{\infty}\frac{I_n(x)}{I_0(x)}\cos(nwt)\right] \tag{36}$$

$$I_{dc} = I_s e^{\frac{qV_{dc}}{kT}} I_0(x) \tag{37}$$

$$V_{dc} = \frac{kT}{q}\ln\left[\frac{I_{dc}}{I_s I_0(x)}\right] \Rightarrow \frac{kT}{q}\ln\left[\frac{I_{dc}}{I_s}\right] + \frac{kT}{q}\ln\left[\frac{1}{I_0(x)}\right] \tag{38}$$

$I_s$ = collector saturation current

$$V_{dc} = V_{dcQ} - \frac{kT}{q} \ln I_0(x) \tag{39}$$

$$i_e(t) = I_{dc}\left[1 + 2\sum_{1}^{\infty} \frac{I_n(x)}{I_0(x)} \cos(nwt)\right] \tag{40}$$

$V_{dcQ}$ and $I_{dc}$ are the operating DC bias voltage and the DC value of the emitter current. Furthermore, the Fourier transform of $i_e(t)$, a current pulse or series of pulses in the time domain yields a number of frequency harmonics common in oscillator circuit designs using nonlinear devices.

The peak amplitude of the harmonic content of the output current is defined as $\left[\frac{I_N(x)}{I_1(x)}\right]$, and the DC offset voltage are calculated analytically in terms of the drive level, as shown in Table 1. It gives good insight of the nonlinearities involved in the oscillator design.

**Table 1: For T=300 K, data are generated at a different drive–level**

| Drive level [x] | Drive-Voltage $\left(\left[\frac{kT}{q}\right] * x\right)$mV | Offset-Coefficient ln[$I_0$(x)] | DC-Offset $\frac{kT}{q}[\ln I_0(x)]$ mV | Fundamental Current 2[$I_1$(x)/$I_0$(x)] | Second-Harmonic [$I_2$(x)/$I_1$(x)] |
|---|---|---|---|---|---|
| 0.00 | 0.000 | 0.000 | 0.000 | 0.000 | 0.000 |
| 0.50 | 13.00 | 0.062 | 1.612 | 0.485 | 0.124 |
| 1.00 | 26.00 | 0.236 | 6.136 | 0.893 | 0.240 |
| 2.00 | 52.00 | 0.823 | 21.398 | 1.396 | 0.433 |
| 3.00 | 78.00 | 1.585 | 41.210 | 1.620 | 0.568 |
| 4.00 | 104.00 | 2.425 | 63.050 | 1.737 | 0.658 |
| 5.00 | 130.00 | 3.305 | 85.800 | 1.787 | 0.719 |
| 6.00 | 156.00 | 4.208 | 206.180 | 1.825 | 0.762 |
| 7.00 | 182.00 | 5.127 | 330.980 | 1.851 | 0.794 |
| 8.00 | 208.00 | 6.058 | 459.600 | 1.870 | 0.819 |
| 9.00 | 234.00 | 6.997 | 181.922 | 1.885 | 0.835 |
| 10.00 | 260.00 | 7.943 | 206.518 | 1.897 | 0.854 |
| 15.00 | 390.00 | 12.736 | 331.136 | 1.932 | 0.902 |

| | | | | | |
|---|---|---|---|---|---|
| 20.00 | 520.00 | 17.590 | 457.340 | 1.949 | 0.926 |

It may be of interest to see the start-up condition of an oscillator; the transient response is shown in Figure 5.

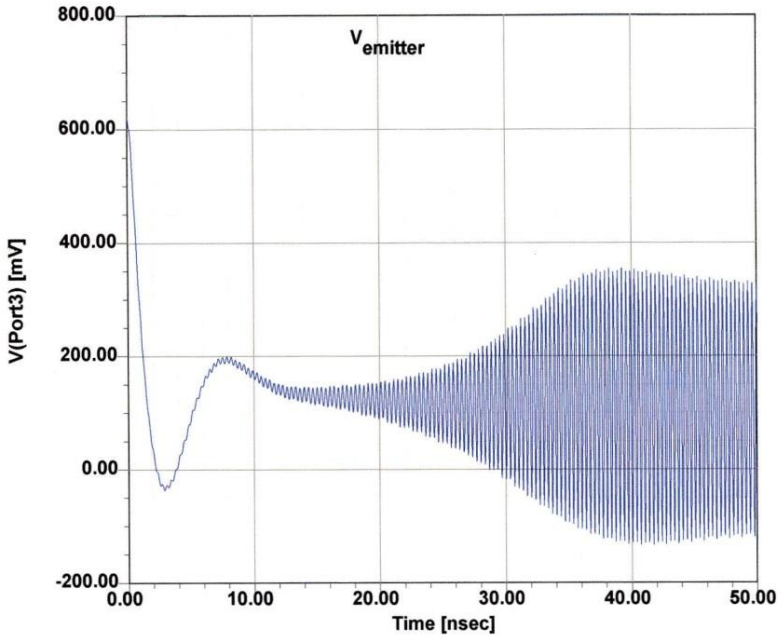


**Figure 5: Example of the transient simulation of a ceramic resonator based high-Q oscillator showing the DC-offset as shown in column 4, Table 1 (The voltage displayed is taken from the emitter)**

**Selecting the right transistor:**

The basic design of a Colpitts oscillator is the same, whether one uses a FET or BJT. Bipolar transistor based oscillators can now easily be designed up to 20GHz. The basic advantage of the bipolar transistor (also known as BIP) is the lower flicker noise corner frequency. Currently transistor chips with $F_{max}$ up to 300GHz are available in the foundry environment, commercially up to about 150GHz. For the purpose of this design synthesis, we have decided to use a BFG520, which is a highly linear transistor. It is validated with a 3-tone test (the typical 2-tone test is easier to meet), as found from the

datasheet; the mixing products are better than -60dB suppressed relative to the carrier. Based on past experience for its good linearity, the BFG520 also has low distortion and, low noise. The key parameters are $V_{CEO}$ = 15V, $I_c$ = 70mA, $P_{tot}$ = 300mW, Noise Figure $F_{min}$ at 350MHz is less than1dB, at 5mA, the associated gain is more than 17dB.

**A Design Example for a 350MHz fixed frequency Colpitts Oscillator**

The following is an exact mathematical solution for designing the 350MHz Colpitts Oscillator.

The circuit consists of the Colpitts configuration following Figure 1c. In order to have enough loop gain, a microwave transistor BFG520 is used. At the proposed starting DC current of 6mA, (being close to the minimum noise figure current and as a first trial to meet the output power), $f_T$ is 6GHz. When selecting a transistor with a higher $f_T$ there is always a possibility of unwanted microwave oscillation and higher flicker noise. When comparing microwave transistors with audio transistors, it becomes apparent that at much lower frequencies there is much less flicker noise contribution. This transistor can safely be operated at 30mA but the rule of thumb is, when using 10% to 15% of $Ic_{max}$, the flicker contribution is much less. For low noise operation, the datasheet indicates 1.1dB spot noise figure at 900MHz at 5mA.

The 350 MHz oscillator, using the bipolar transistor BFG520, is designed based on analytical equations and is later verified with simulation results. Based on the output power requirement and harmonics at a given load, the drive level is fixed. The normalized drive level (of x = 15) is chosen to allow adequate drive level to sustain oscillation and yet, not to produce excessive harmonic content. Figure 6, shows the values of the optimized circuit. While simulating for a series resonant configuration, the value of $C_p$ = 8.2fF, was used as a place-holder, based on impedance considerations. $C_p$ was set to 8.2pF for parallel resonant configuration, the value of L = 21nH, and $C_c$ = 3.3pF was set

to achieve oscillation at 350MHz. Experimenting with the simulation, it turns out that '$L_b$' set to 0.5uH gives a much better phase noise, about 10dB better at 100Hz offset, but this could not be verified yet in a real circuit.

The output power is taken from the collector and following is the design procedure. The goal is to obtain an output power over 10dBm, using a simple design for good understanding.

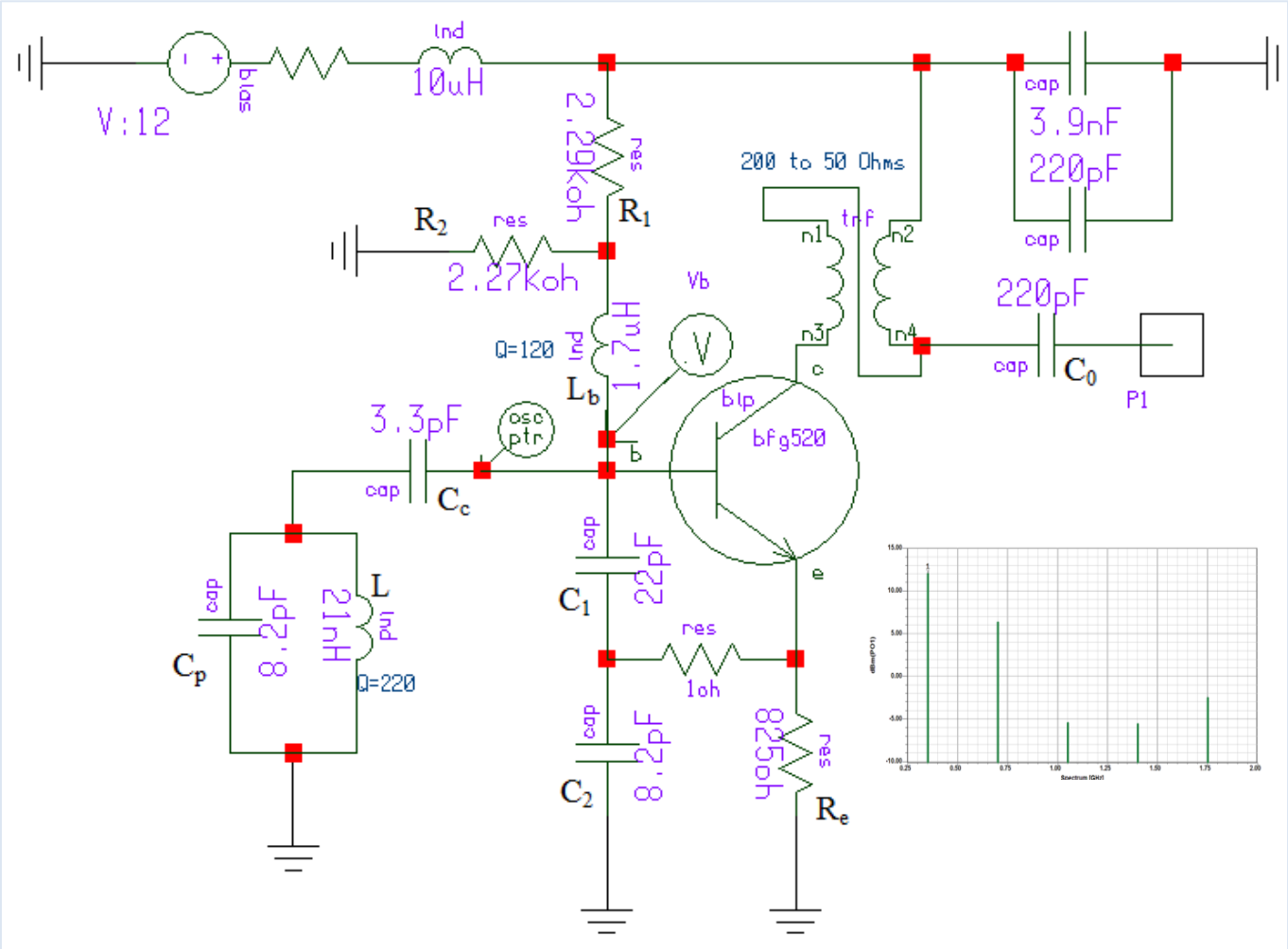


**Figure 6: Design of 350MHz Colpitts Oscillator – Optimized for phase noise**

**Step 1:**

The normalized drive level will be set at 15, for which the fundamental peak current

$I_1$ *(fundamental)* = $1.932 I_{dc}$ (is given from table 1).

$I_1$ is the fundamental current specified by the output power needed for the designated load.

The primary impedance of the transformer is 200Ω and we calculate the RF voltage for $R_L = 200\Omega$ and for a output power of $P_{out} \approx 11$ dBm ≈ 14mW

$V_{out} = \sqrt{P_{out}(mW) \times 2R_L} = \sqrt{14 \times 10^{-3} \times 2 \times 200} = 2.37V$ (No saturation voltage assumed! This results in slight variation between calculated, simulated and measured values of Pout.) (41)

$$I_1 = \frac{V_{out}}{200} = \frac{2.37}{200} \cong 11.85mA \quad (42)$$

$$I_e = I_{dc} = \frac{I_1}{1.932} = \frac{11.85}{1.932} = 6.13mA \quad (43)$$

**Step 2: Biasing**

The transistor uses a 12V power supply and an 825Ω emitter resistor at ~6mA, resulting in ~5V drop, so the transistor can afford a large voltage swing between base and ground. This reduces flicker noise (resistive feedback) and distortion. The base voltage divider, for reasons pertaining to temperature stability uses a higher than normal dc current, is isolated from the base using a RF choke. Frequently, in designs, this circuit trick is not used.

$$V_b = I_e \left[ R_e + \frac{R_e}{\beta + 1} \right] + V_{be} = 5.96V \quad (44)$$

$\beta$ is assumed to be around 100 and $V_{be}$ is approximately 0.8V.Bias resistor $R_1$ and $R_2$ is given as

$$V_b = \frac{R_2}{R_1 + R_2} V_{cc} = 5.96V \Rightarrow \frac{R_1}{R_2} \approx 1 \quad (45)$$

$$R_1 = 2270\Omega \tag{46}$$

$$R_2 = 2290\Omega \tag{47}$$

$$V_{cc} = 12V \tag{48}$$

Resistor Bias current is ~2.6mA ($V_{cc}/(R_1+R_2)$)

Base current is 43$\mu$A, so the safety factor is $2.6/0.043 \cong 60$

**Step 3: Determination of the large signal transconductance**

Based on the table above, and x=15, the "DC transconductance" equals

$$Y_{21} = \left.\frac{I_1}{V_1}\right|_{fundamental-freq} = \frac{1.932 I_{dc}}{1000mV} = \frac{11.85mA}{1000mV} \cong 12mS \tag{49}$$

This is the DC transconductance, meaning the frequency dependence has not been considered.

An analysis of the transistor shows that the small signal transconductance at 6mA (dc) is about 6×39 ≈ 240mS. At 350MHz this reduces itself to 200mS down from 240mS. This is valid only if the transistor does not have any emitter feedback. In the case of the Colpitts oscillator we have an emitter resistor which reduces the transconductance; therefore we have to multiply $Y_{21}$ with

$$\left(\frac{1}{(1/g_m) + R_e}\right) \tag{50}$$

The resulting large signal loop transconductance $Y_{21L}$ is $\frac{1}{(\frac{1}{12\times10^{-3}}) + 825)} \cong 1.1mS$, which is an acceptable approximation, as the exact value of x is about 20 (see simulation results, Figure 9) [Ref. 26, pg.177].

Based on Kirchhoff's law, the following set of equations can be used to determine the feedback factor '$n$'.

$Y_{21L} = 1.1mS$ (DC Transconductance – No high frequency effects included) where $\alpha = 0.99$

The oscillator circuit with passive component parameters is shown in Figure 7a.

**Table 2: Large signal transconductance as a function of Drive level based on Bessel function Calculations - $G_m(x)/g_m=2[I_1(x)/xI_0(x)]$ vs. the drive level = x.**

| Drive level: x | $G_m(x)/g_m=2[I_1(x)/xI_0(x)]$ |
|---|---|
| 0.00 | 1 |
| 0.50 | 0.970 |
| 1.00 | 0.893 |
| 2.00 | 0.698 |
| 3.00 | 0.540 |
| 4.00 | 0.432 |
| 5.00 | 0.357 |
| 6.00 | 0.304 |
| 7.00 | 0.264 |
| 8.00 | 0.233 |
| 9.00 | 0.209 |
| 10.00 | 0.190 |
| 15.00 | 0.129 |
| 20.00 | 0.0975 |
| 25.00 | 0.075 |

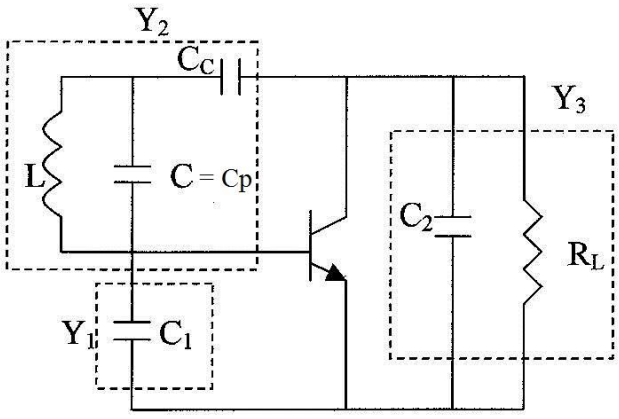


**Figure 7a: Oscillator circuit with the passive components $Y_1$, $Y_2$, and $Y_3$**

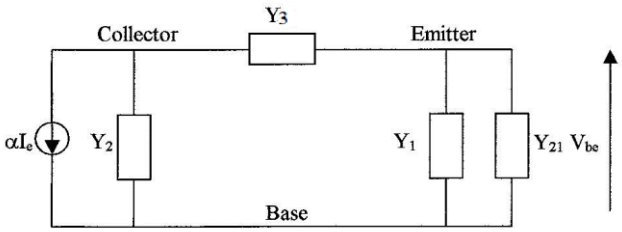


**Figure 7b: Equivalent oscillator circuit for the analysis of the transformed conductance seen by the**

**current source**

Where,

$$Y_1 = G_1 + jB_1 \Rightarrow j\omega C_1 \text{ For } G_1 = 0 \quad (51\text{-a})$$

$$Y_2 = G_2 + jB_2 \Rightarrow G_2 + j\left[\frac{(\omega^2 LC - 1)\omega C_c}{\omega^2 L(C_c + C) - 1}\right]; \quad (51\text{-b})$$

$G_2$ = loss parameter/load conductance of the resonator connected parallel to the resonator component $C_1$, $C_2$ and $L$, respectively.

$$Y_3 = G_3 + jB_3 \Rightarrow G_3 + j\omega C_2; \quad (51\text{-c})$$

$G_3$ = conductance of the bias resistor placed across $C_2$, $1/R_L$ in Figure 7a.

The large-signal transconductances $Y_{21}$ and $G_1$ are transformed to the current source through the voltage divider $\frac{V_{eb}}{V_{cb}}$. The voltage $V_{eb}$ must be added to $V_{ce}$ to calculate the transformation ratio, which is also inverse of the feedback factor and can be written as $\frac{V_{eb}}{V_{cb}} = \frac{C_2}{C_1 + C_2} = \frac{1}{n}$ (51-d)

And $\frac{V_{ce}}{V_{cb}} = \frac{C_1}{C_1 + C_2} = \frac{n-1}{n}$ (51-e)

The conductance $G_2$ is already in parallel with the current source so it remains unchanged. The factor "n" represents the ratio of the collector-base voltage to the emitter-base voltage at the oscillator resonant frequency.

$$G_1 \rightarrow \frac{G_1}{n^2} \quad (51\text{-f})$$

$$Y_{21} \rightarrow \frac{Y_{21}}{n^2} \Rightarrow \frac{G_m}{n^2} \tag{51-g}$$

$$G_3 \rightarrow \left[\frac{n-1}{n}\right]^2 G_3 \tag{51-h}$$

$G_2$ remains constant

The transformed conductance is proportional to the square of the voltage ratios given in Equations (51-d) and (51-e), producing a total conductance as seen by the current source at resonance as

$$G_{total} = G_2 + \frac{G_m + G_1}{n^2} + \left[\frac{n-1}{n}\right]^2 G_3 \tag{51-i}$$

For sustained oscillation, the closed loop gain at resonance is given as

$$\left[\frac{\left(\frac{V_{be} Y_{21} \alpha}{nG_{total}}\right)}{V_{be}}\right] = 1 \Rightarrow nG_{total} = Y_{21}\alpha \tag{51-j}$$

$$\frac{Y_{21}}{nG_{total}} = \frac{1}{\alpha} \Rightarrow \frac{Y_{21}}{nG_{total}} > 1 \tag{51-k}$$

$\alpha$ is assumed to be 0.0.99 and variation in the value of $\alpha$ does not influence the expression above greatly. Rearranging the device conductance and circuit conductance, the general oscillator equation, after multiplying (51-i) with *n* on both sides, is written as

$$nG_{total} = n\left[G_2 + \frac{Y_{21} + G_1}{n^2} + \left(\frac{n-1}{n}\right)^2 G_3\right] \tag{51-l}$$

$$Y_{21}\alpha = n\left[G_2 + \frac{Y_{21} + G_1}{n^2} + \left(\frac{n-1}{n}\right)^2 G_3\right] \Rightarrow \left[\frac{-(1-n\alpha)}{n^2}\right] Y_{21} = \left[G_2 + \frac{G_1}{n^2} + \left(\frac{n-1}{n}\right)^2 G_3\right] \tag{51-m}$$

$$n^2(G_2+G_3)-n(2G_3+Y_{21}\alpha)+(G_1+G_3+Y_{21})=0 \tag{51-n}$$

$$n=\frac{(2G_3+Y_{21}\alpha)\pm\sqrt{(2G_3+Y_{21}\alpha)^2-4(G_2+G_3)(G_1+G_3+Y_{21})}}{2(G_2+G_3)} \tag{51-o}$$

$$n_1=\frac{(2G_3+Y_{21}\alpha)}{2(G_2+G_3)}+\frac{\sqrt{(2G_3+Y_{21}\alpha)^2-4(G_2+G_3)(G_1+G_3+Y_{21})}}{2(G_2+G_3)} \tag{51-p}$$

$$n_2=\frac{(2G_3+Y_{21}\alpha)}{2(G_2+G_3)}-\frac{\sqrt{(2G_3+Y_{21}\alpha)^2-4(G_2+G_3)(G_1+G_3+Y_{21})}}{2(G_2+G_3)} \tag{51-q}$$

From the quadratic equation above, the value of the factor n can be calculated, and thereby, an estimation of the capacitance can be done a priori.

To ensure higher loop gain, $n_1$ is selected from $n_{max}[n_1, n_2]$.

Once the value of n is fixed, then the ratio of the capacitance is calculated as

$$\frac{C_2}{C_1+C_2}=\frac{1}{n} \tag{51-r}$$

$$C_2=\frac{C_1}{n-1}\Rightarrow\frac{C_1}{C_2}=n-1 \tag{51-s}$$

If $G_3$ and $G_1$ are zero then the quadratic equation (51-n) reduces to

$$n^2G_2-nY_{21}\alpha+Y_{21}=0 \tag{51-t}$$

$$Y_{21}\cong\frac{n^2}{1-n}G_2\Rightarrow Y_{21}=\left[\frac{n^2}{1-n}\right]\frac{1}{R_P} \tag{51-u}$$

$$\frac{Y_{21}R_P}{n}=\frac{n}{1-n} \tag{51-v}$$

$$R_P=\frac{1}{G_2},\qquad \frac{Y_{21}R_P}{n}\rightarrow Loop\ Gain \tag{51-w}$$

$$\textit{Loop Gain}\ \ \frac{Y_{21}R_P}{n} \to 1 \tag{51-x}$$

From equation (51-r) and (51-u)

$$Y_{21} \Rightarrow G_m(x) = \frac{1}{R_P}\frac{[C_1 + C_2]^2}{C_1 C_2} \tag{51-y}$$

The quadratic equation for *n* (from (51-n)) is reduced to

$$n^2(G_3) - n(2G_3 + Y_{21}\alpha) + (G_3 + Y_{21}) = 0 \tag{52-a}$$

$$G_3 = \frac{1}{R_e} = \frac{1}{825} = 1.21mS$$

$$n^2(1.21) - n(2\times 1.21 + 1.1\times 0.99) + (1.21 + 1.1) = 0 \tag{52-b}$$

$$1.21n^2 - 3.514n + 2.313 = 0 \tag{52-c}$$

$$n = \frac{3.514 \pm \sqrt{(3.514)^2 - 4\times 1.21\times 2.313}}{2\times 1.21} \tag{53}$$

$$n \Rightarrow n_1 = 1.888 and\ n_2 = 1.01 \tag{54}$$

The higher value of the transformation factor, *n*, is selected as *n* = 1.888.

The ratio for the values of $C_1$ and $C_2$ is calculated as

$$\frac{C_2}{C_1 + C_2} = \frac{1}{n} \Rightarrow C_2 = \frac{C_1}{n-1} \tag{55}$$

$$C_2 = \frac{C_1}{n-1} = \frac{C_1}{0.888} \Rightarrow \frac{C_1}{C_2} \cong 0.9 \approx 1 \tag{56}$$

The ratio of the capacitor $C_1$ to $C_2$ is 1. For larger transconductance, $Y_{21}$, $(C_1/C_2) > 1$

**A discussion about drive level and noise:**

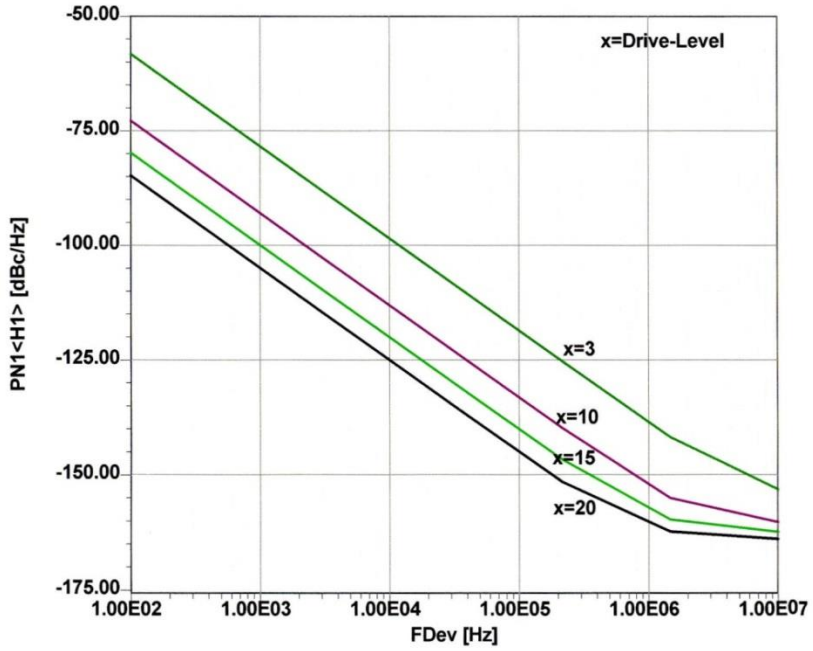


**Figure 8: Example for the single sideband phase noise as a function of the normalized drive level x for a high Q 1GHz oscillator**

The plot in Figure 8 [5] shows the impact of the normalized drive level 'x' on the phase noise. The exact values have to be assessed for individual circuits, but the general trend follows the plot shown.

In Figure 9, x=1 is the linear case (Class A – operation) and the values above x=15 produce narrow pulses. Class A operation gives higher output power but is not optimized for phase noise. However at higher drive levels, the transistor is "ON" for shorter duration, thus less loading and better phase noise, but at the cost of lower power output.

If the transistor is overdriven at the base, the collector current folds back (dip) and the actual current gain falls to values of 1.4 in our case (From Figure 9).

For the uncompressed current gain $(Y_{21}/Y_{11}) \approx (C_2/C_1) \approx 270pF/10pF$, the circuit will actually oscillate but does not have acceptable phase noise (low value of x, n=28, where $n = (C_1/C_2) +1$).

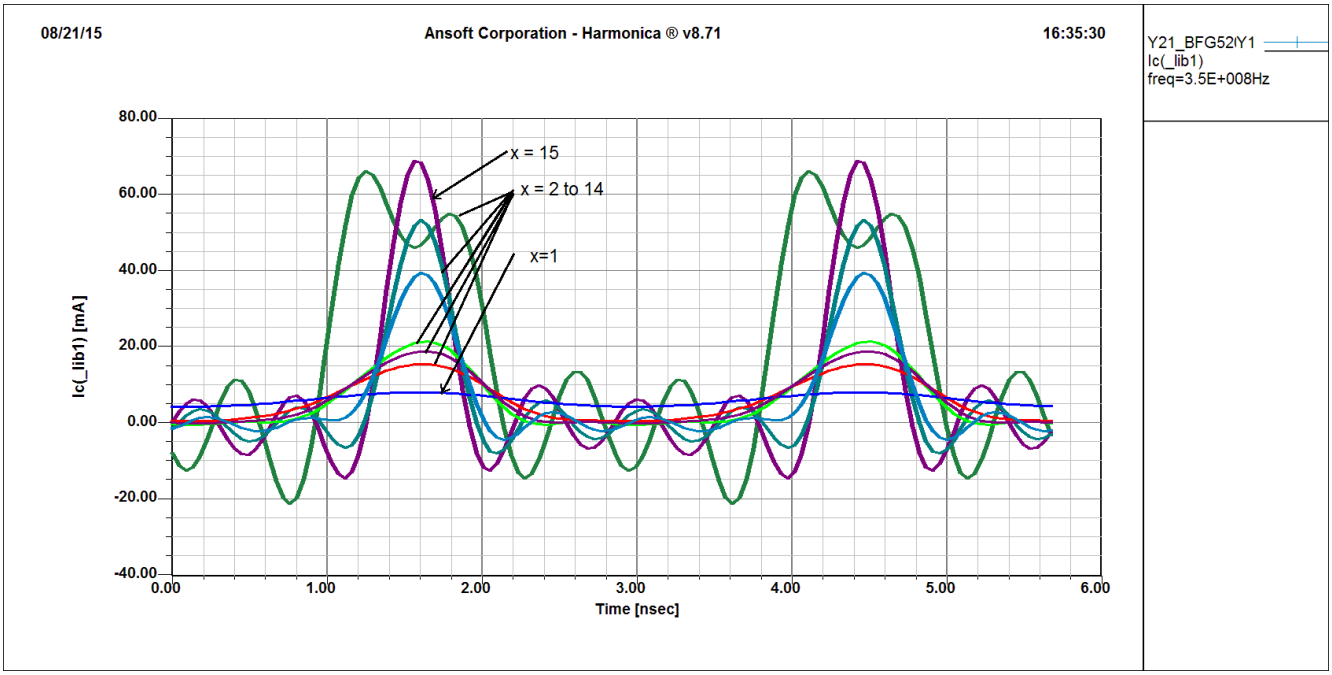


**Figure 9: Shows $I_c$ as a function of drive level. X**

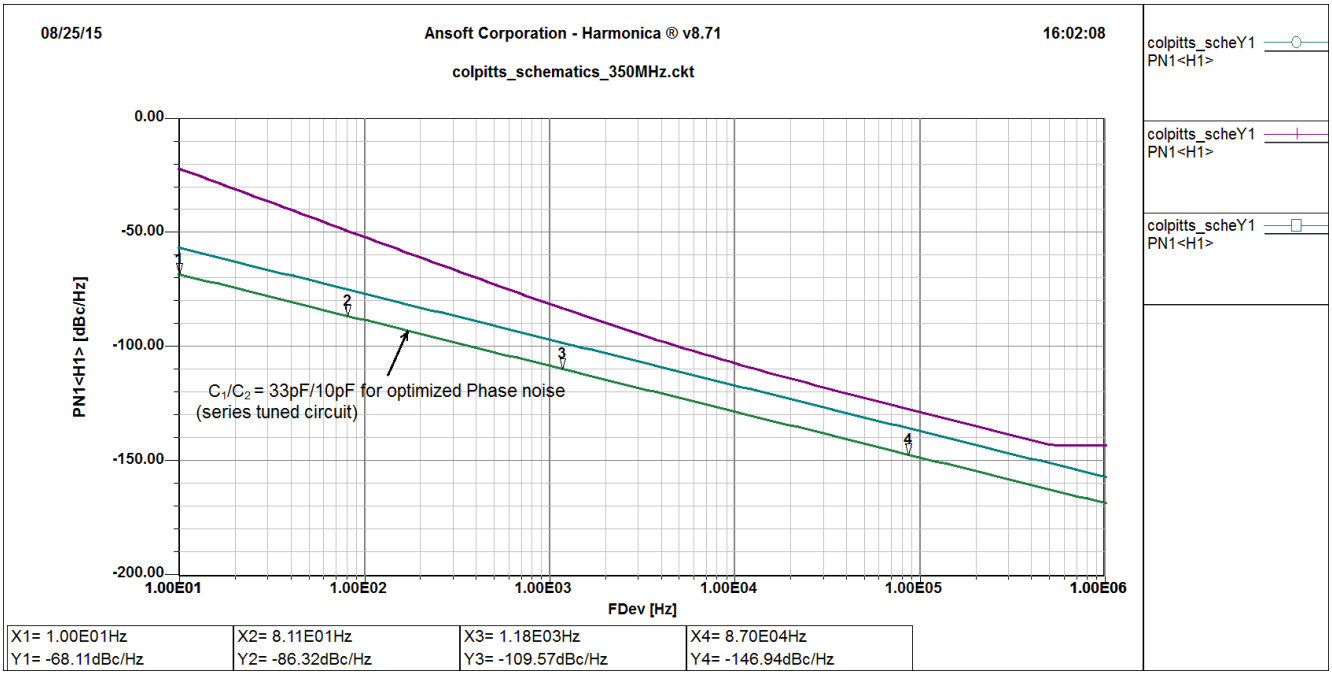


**Figure 10: Optimization of Phase Noise for the series tuned circuit**

By changing the capacitors $C_1/C_2$ to 33pF/10pF, n = 4.3, the phase noise performance is optimized, as shown in Figure 10. This circuit is a series tuned oscillator and now we move on to a high Q (from

Q=220 to Q=450) circuit, where the resonator is loosely coupled to the transistor. The tuned circuit consists of a 22nH inductor and 8.2pF capacitor. The following shows the design calculation for the parallel tuned circuit as found in ceramic resonator based oscillators.

The quality factor of the inductor is assumed 60 at 350 MHz, a low Q case.

The value of inductor is obtained as

$$Q_T = \frac{R_P}{\omega_0 L} \Rightarrow L = \frac{3649}{60 \times \omega_0} \qquad \text{(where } R_p \text{ is calculated using } \; G_m(x) = \frac{1}{R_P}\frac{C_1}{C_2}\left[1+\frac{C_2}{C_1}\right]^2 \tag{57}$$

$$L = \frac{3649}{60 \times 2\pi \times 350 \times E6} \approx 27nH \tag{58}$$

$$\omega = \sqrt{\frac{1}{L}\left[\frac{1}{C_1}+\frac{1}{C_2}\right]} \tag{59}$$

$$\omega^2 = \frac{1}{L}\left[\frac{1}{C_1}+\frac{1}{C_2}\right] = \frac{C_1 + C_2}{LC_1C_2} \tag{60}$$

The value of the capacitor is determined as

$$C_2 = \frac{2.55}{\omega^2 \times 17E - 9} \approx 14pF \tag{61}$$

$$C_1 \approx C_2 \approx 14pF \tag{62}$$

Taking into consideration the actual parasitics and RF parameters of the transistor, the optimized values are $C_1$ =12pF and $C_2$ = 8.2pF

**Step 4: Calculation of the coupling capacitor $C_c$:** [5, eqn (C-23)]

The expression for the coupling capacitor is

$$\frac{C}{10} > C_C > \left\{\frac{(\omega^2 C_1 C_2)(1+\omega^2 Y_{21}^2 L_P^2)}{[Y_{21}^2 C_2 - \omega^2 C_1 C_2)(1+\omega^2 Y_{21}^2 L_P^2)(C_1 + C_P + C_2)]}\right\} \tag{63}$$

$C_c$ = 3.3pF (64)

**Step 5: Calculation of the Phase Noise of the Colpitts Oscillator:**

The mathematical expression of the phase noise of a Colpitts Oscillator is [5, pp180].

$$L(\omega) = 10Log\left\{\left[4kTR + \left[\frac{4qI_c g_m^2 + \frac{K_f I_b^{AF}}{\omega} g_m^2}{\omega_0^2 C_1^2 (\omega_0^2 (\beta^+)^2 C_2^2 + g_m^2 \frac{C_2^2}{C_1^2})}\right]\right]\left[\frac{\omega_0^2}{4\omega^2 V_{cc}^2}\right]\left[\frac{1}{Q^2} + \frac{[C_1 + C_2]^2}{C_1^2 C_2^2 \omega_0^4 L^2}\right]\right\} \quad (65)$$

where

$$\beta^+ = \left[\frac{Y_{21}^+}{Y_{11}^+}\right]\left[\frac{C_1}{C_2}\right]^p$$

$g_m = \left[Y_{21}^+\right]\left[\frac{C_1}{C_2}\right]^q$; values of *p* and *q* depends upon the drive level (x)

$Y_{21}^+$, $Y_{11}^+$ = large signal [Y] parameter of the active device

$K_f$ = flicker noise coefficient

*AF* = flicker noise exponent

*£(ω)* = ratio of sideband power in a 1Hz BW at $\omega$ to total power in dB

$\omega$ = frequency offset from the carrier

$\omega_0$ = center frequency

$Q_L$ = loaded *Q* of the tuned circuit

$Q_O$ = unloaded *Q* of the tuned circuit

*kT* = $4.1 \times 10^{-21}$ at 300 K (room temperature)

*R* = equivalent loss resistance of the tuned resonator circuit

$I_c$ = RF collector current

$I_b$ = RF base current

$V_{cc}$ = RF collector voltage

$C_1$, $C_2$ = feedback capacitor

Using a Mathcad calculation, we obtain the following results as shown in Figure 11, [5, eqn 8-109], which compares well with the measured data.

**Phase Noise Equation**

$Ic := 6.2 \cdot 10^{-3}$ $Ib := 43.2 \cdot 10^{-6}$ $L := 22 \cdot 10^{-9}$ $C_1 := 12 \cdot 10^{-12}$ $C_2 := 8.2 \cdot 10^{-12}$ $C_c := 3.3 \cdot 10^{-12}$

$K := 1.3806 \cdot 10^{-23}$ $T := 300$ $KT := 4.143 \cdot 10^{-21}$ $R := 0.3$ $Kf := 1 \cdot 10^{-7}$ $AF := 2$

$Q := 60$ $Vcc := 12$ $f := 350 \cdot 10^{6}$ $w0 := 2 \cdot \pi \cdot f$ $\beta := 140$

$r_e := \frac{26 \cdot 10^{-3}}{Ic}$ $gm1 := \frac{1}{r_e}$ $gm1 = 0.238$ $q := 1.602 \cdot 10^{-19}$ $i := 0..7$ $fo_i := 10^i$

$wo_i$ is the frequecny offset from the carrier $wo_i := 2 \cdot \pi \cdot fo_i$

$$Lw_i := 10 \cdot \log\left[\left[4 \cdot KT \cdot R + \left[\frac{4 \cdot q \cdot Ic \cdot gm1^2 + \frac{Kf \cdot Ib^{AF}}{wo_i} \cdot gm1^2}{(w0)^2 \cdot C_1^2 \cdot \left[(w0)^2 \cdot \beta^2 \cdot C_2^2 + gm1^2 \cdot \frac{C_2^2}{C_1^2}\right]}\right]\right] \cdot \left[\frac{w0^2}{4 \cdot (wo_i)^2 \cdot Vcc^2} \cdot \left[\frac{1}{Q^2} + \frac{(C_1 + C_2)^2}{C_1^2 \cdot C_2^2 \cdot (w0)^4 \cdot L^2}\right]\right]\right]$$

| $fo_i$ | $Lw_i$ |
|---|---|
| 1 | -5.227 |
| 10 | -35.222 |
| 100 | -65.165 |
| $1 \cdot 10^3$ | -94.633 |
| $1 \cdot 10^4$ | -121.303 |
| $1 \cdot 10^5$ | -143.272 |
| $1 \cdot 10^6$ | -163.529 |
| $1 \cdot 10^7$ | -183.555 |

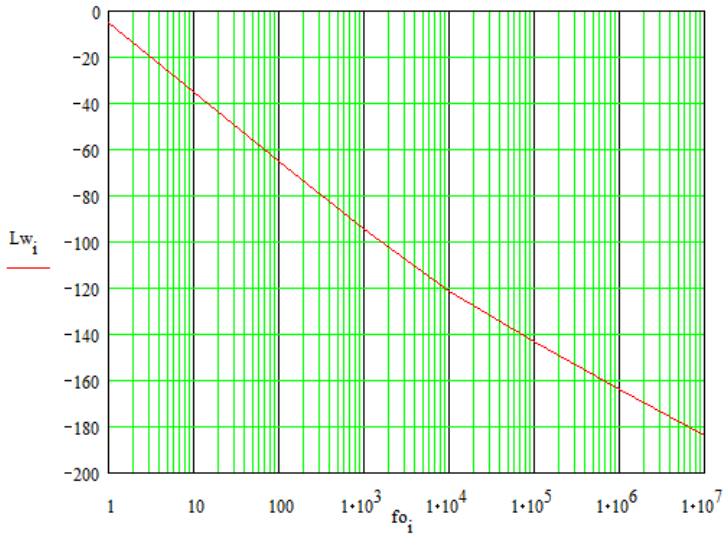


**Figure 11: Mathcad calculation for phase noise**

**Measured results for a 350MHz Oscillator:**

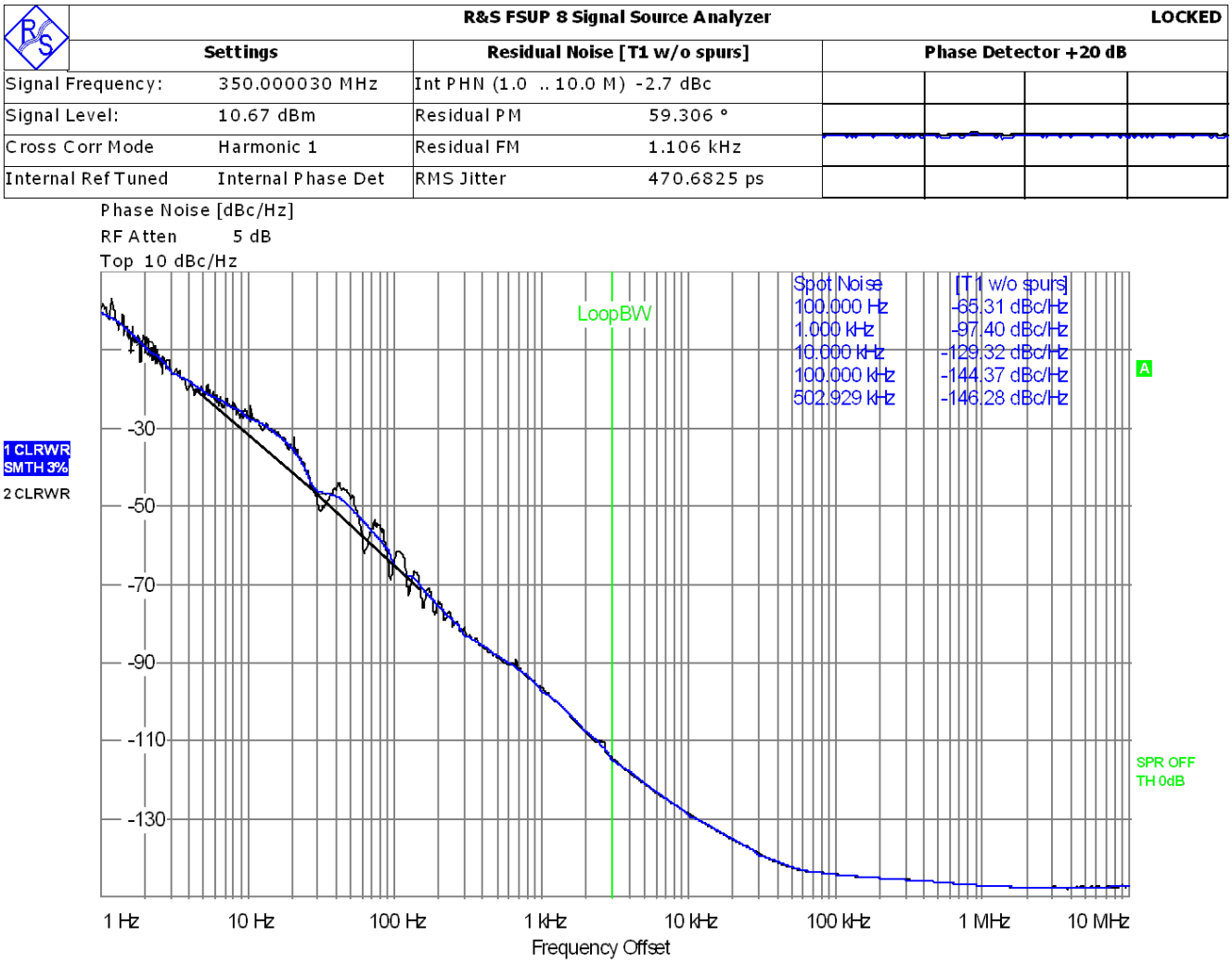


**Figure 12: Measured Phase noise result for 350MHz Oscillator**

The measured phase noise of the oscillator shown in Figure 12 is not quite comparable with the mathematics because it has a two stage buffer amplifier which isolates the oscillator from the output termination. This explains the limit of -146dBc/Hz at far-offset. At close-in, the phase noise is influenced by an AFC circuit. The real comparison should be done between 10Hz and 10 kHz offsets.

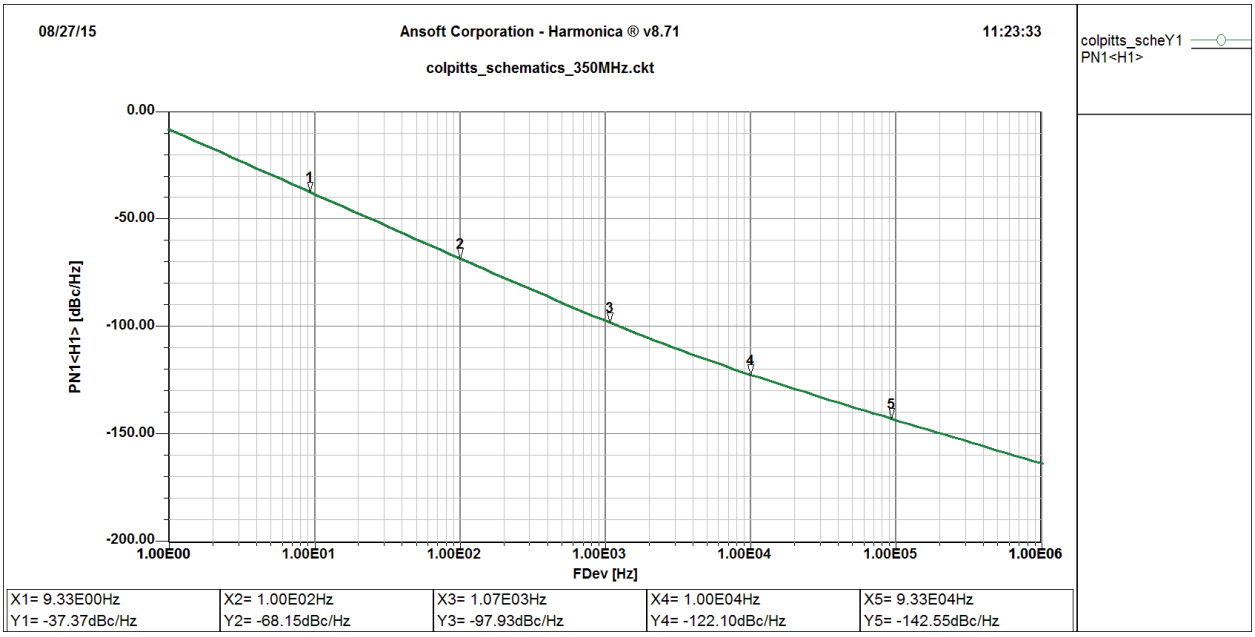


**Figure 13a: Simulated Phase Noise for the 350MHz Parallel Tuned Colpitts configuration**

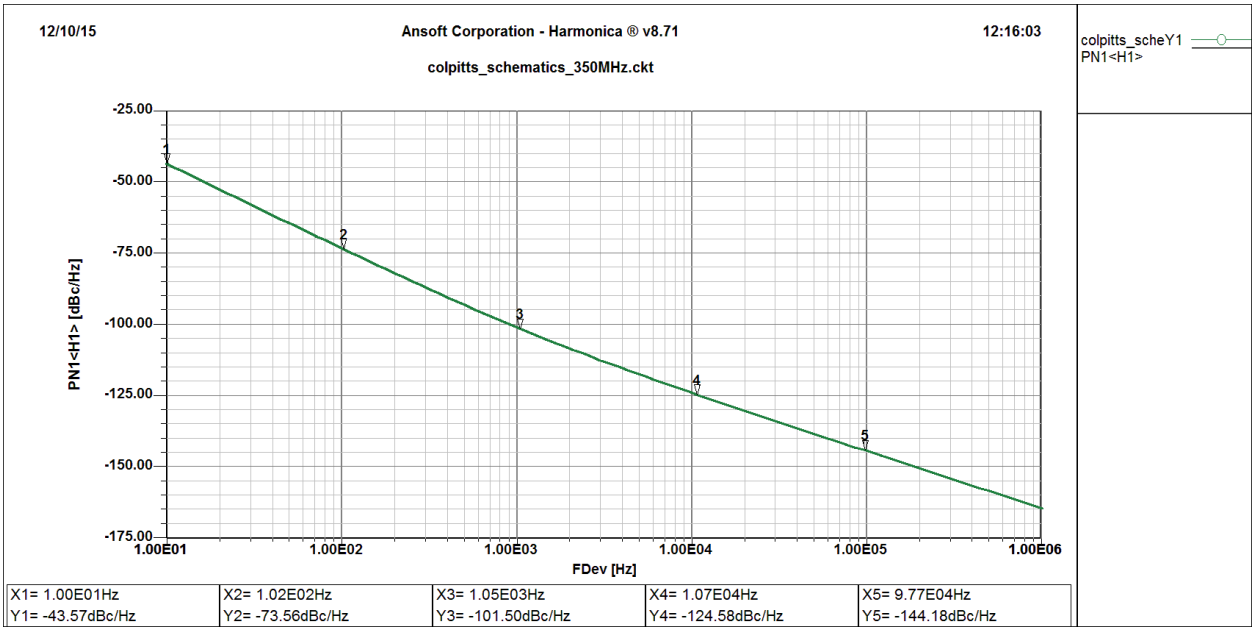


**Figure 13b: Optimized - Simulated Phase Noise for the 350MHz Parallel Tuned Colpitts configuration**

In order to optimize the phase noise for this type of oscillator,), using discrete components, the selection of the following set of values: $C_p$ = 8.2pF, L=21nH, $C_1$=22pF, $C_2$=8.2pF, $C_c$=3.3pF improved the phase noise from -122dBc/Hz to -125dBc/Hz at 10 kHz offset. This is a result of trial-and-error, as

we do not know all the parasitics. Figure 13a shows the simulated phase noise plot and Figure 13b shows further improvement after optimizing the circuit for phase noise.

If we replace the parallel tuned circuit with a ceramic resonator (at this frequency range, Ɛr will be 88, the L/C ratio will be 0.048nH/pF vs. 2.44 nH/pF in case of discrete components used in our case), and the simulated phase noise is 105dBc/Hz at 10 kHz offset.

**Note**: ***This is due to the fact that the characteristic impedance of a ceramic resonator is much lower, than the discrete case***. $Z_0 = 60\Omega \frac{1}{\sqrt{\varepsilon_r}} \ln \frac{D}{d}$ (Where D = outer diameter and d= inner diameter of the ceramic resonator [[12], pp 754]. The prediction agrees well with the measured phase noise [[12], Fig (5-37)].

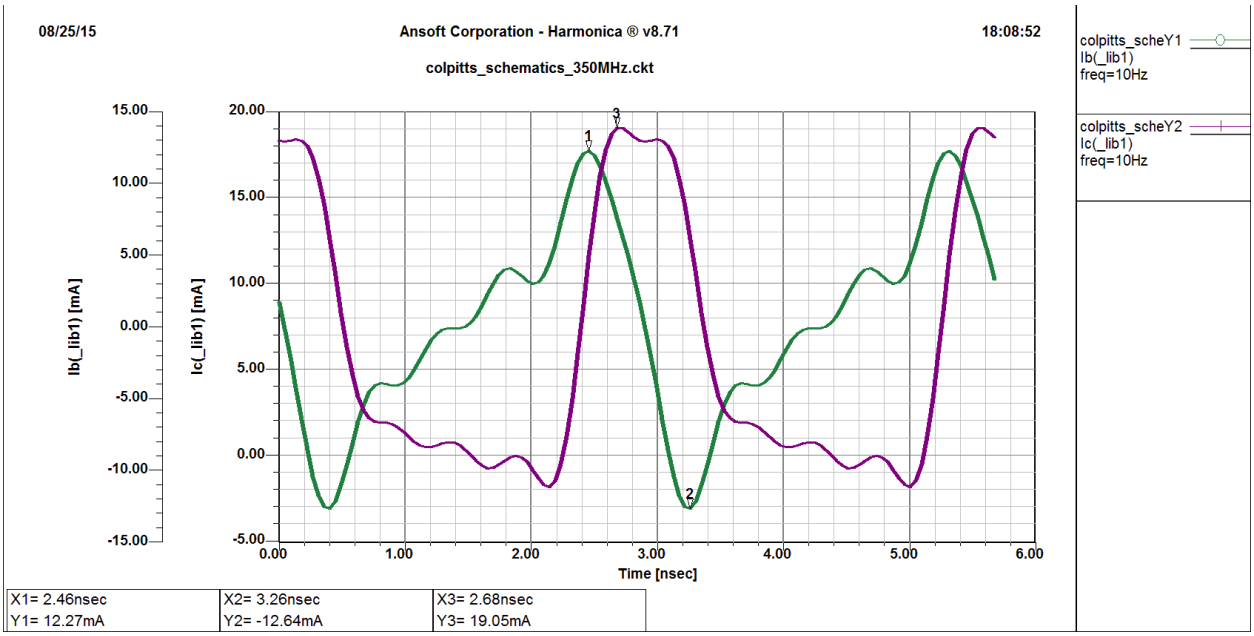


**Figure 14: showing $Y_{21}/Y_{11}$ large signal condition**

Figure 14 shows the plots of the collector and base currents $I_c$ and $I_b$ for the optimized case ($C_p$=8.2pF, L=21nH (Q=60 at 350MHz), $C_c$=3.3pF, $C_1$=12pF, $C_2$=8.2pF).

From the plot in Figure 14, we can determine that the ratio of large signal $(Y_{21}/Y_{11}) = \beta = 1.4$. The next critical parameter, shown in Figure 15 is for the normalized drive level (x) is $V_1/(kT/q)$.

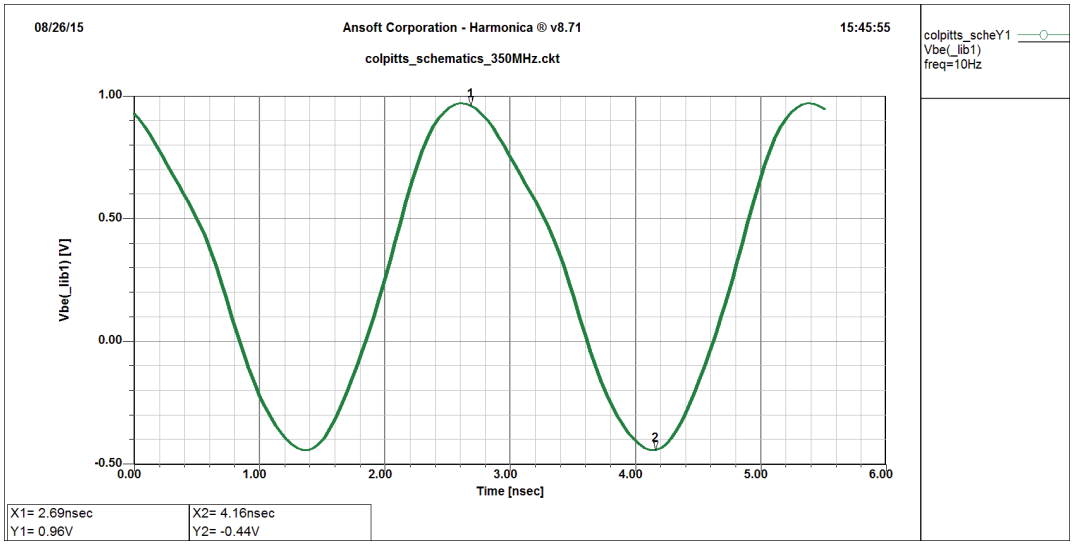


**Figure 15: $V_{be}$ – to calculate the drive level**

From the Figure 15, the RMS value of $V_{be}$ is used to determine the approximate drive level.

$$\text{Since } V_{be} = V_1, \text{ drive level (x)} \approx \frac{500\, mV_{rms}}{26\, mV} \approx 20 \qquad (66)$$

A table of normalized transconductance as a function of the drive level including the large values is given in Table 2 [5].

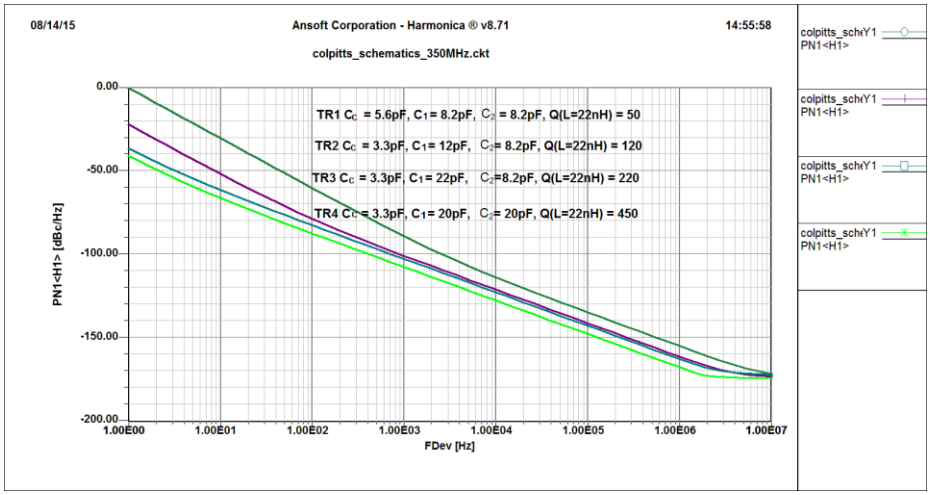


**Figure 16: Optimized phase noise for different values of Inductor Q**

Figures 16 and 17, show the phase noise variation with variation in Q (L=22nH) in the LC resonator. The output power, collector current, and base voltage ($V_b$) and ($V_{be}$) plots are also shown for the same combination.

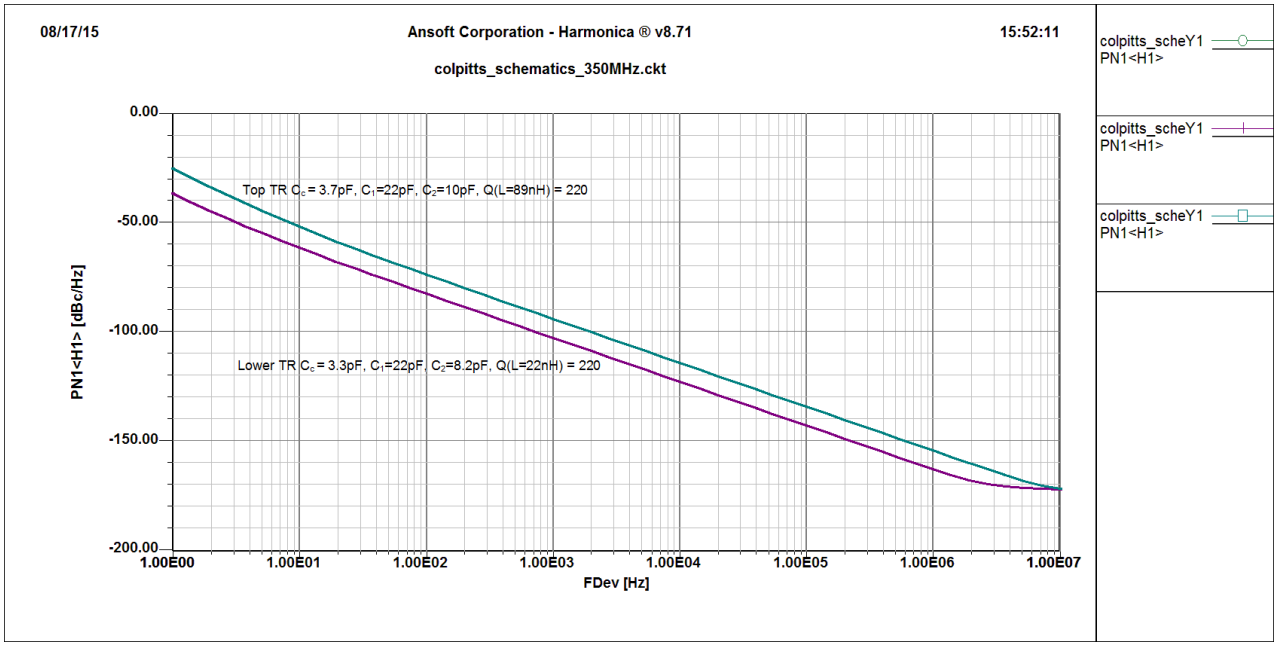


**Figure 17: Results of Series and Parallel tuned circuits for same value of Inductor Q**

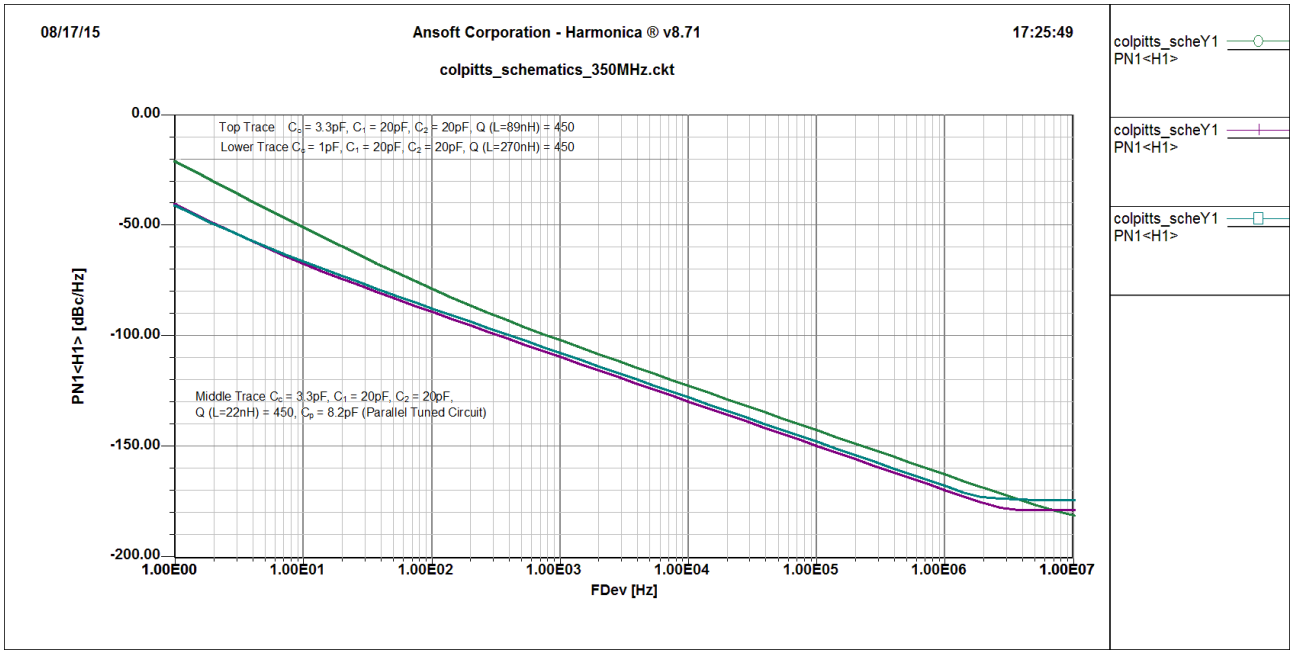


**Figure 18: Results of Series and Parallel tuned circuits for higher value of Inductor Q**

The parallel tuned circuit shows better phase noise performance, as seen in Figure 18, due to the fact that the rate of change of reactance in a parallel tuned circuit is significantly larger than in a simple series tuned oscillator.

**1/f Noise:**

The electrical properties of surfaces or boundary layers are influenced energetically by states, which are subject to statistical fluctuations and therefore, lead to the flicker noise or 1/*f* noise for the current flow.

1/*f* - noise is observable at low frequencies and generally decreases with increasing frequency *f* according to the 1/*f* - law until it will be covered by frequency independent mechanism, like thermal noise or shot noise.

**Example:** The noise for a conducting diode is bias dependent and is expressed in terms of AF and KF.

$$\langle i_{Dn}^2 \rangle_{AC} = 2qI_{dc}B + KF\frac{I_{DC}^{AF}}{f}B$$

- The AF is generally in range of 1 to 3 (dimensionless quantity) and is a bias dependent curve fitting term, typically 2.
- The KF value is ranging from $10^{-12}$ to $10^{-6}$, and defines the flicker corner frequency. [32]

One of the important characteristics for device evaluation and selection is 1/f noise, which is a function of the active device characteristics and a major contributor to phase noise, especially in applications such as VCOs [5, 20]. In an oscillator, 1/f noise that is present in transistors at low frequencies is upconverted and added to the phase noise around the carrier signal. Hence, proper characterization of 1/f noise and its effects on phase noise is an important topic. In addition, 1/f noise is not solely an active device phenomenon. Passive devices such as carbon resistors, quartz resonators, SAW devices, and ceramic capacitors are among devices that show presence of this phenomenon when used as part of

low-noise electronic systems. Generally, 1/f noise is present in most physical systems and many electronic components [19, 22, 23].

Flicker noise in BJTs is also known as 1/f noise because of the 1/f slope characteristics of the noise spectra. This noise is caused mainly by traps associated with contamination and crystal defects in the emitter-base depletion layer. These traps capture and release carriers in a random fashion. The time constants associated with the process produce a noise signal at low frequencies. The flicker noise spectral density is given by:

$$S(f)df = (KF)IB^{AF}df/Fc \tag{67}$$

where:

KF = flicker noise constant

AF = flicker noise exponent

IB = DC base current

Fc = flicker noise corner frequency

The measured flicker corner frequency, $F_{meas}$, is determined by noting the intersection of the 1/f noise spectrum and the white noise spectrum. This intersection is where the measured flicker noise power and the white noise power are equal. To determine $F_{bn}$, the intrinsic base flicker noise corner, requires solving the following equation [20, 21]:

$$F_{bn} = F_{meas}\,[1 + 1/\beta + 2V_{th}G_{in}/IB] \tag{68}$$

where:

$F_{bn}$ = intrinsic base flicker noise corner

$F_{meas}$ = measured flicker corner

$\beta$ = collector-base current gain

$V_{th}$ = thermal voltage = kT/q

$G_{in}$ = external input conductance

IB = DC base biasing current

The equation for the intrinsic base flicker corner modifies the measured flicker corner to account for the input conductance, base current, and DC current gain of the device. The formula for $F_{bn}$ is valid provided the measured output noise characteristics are dominated by the base flicker and base shot noise sources.

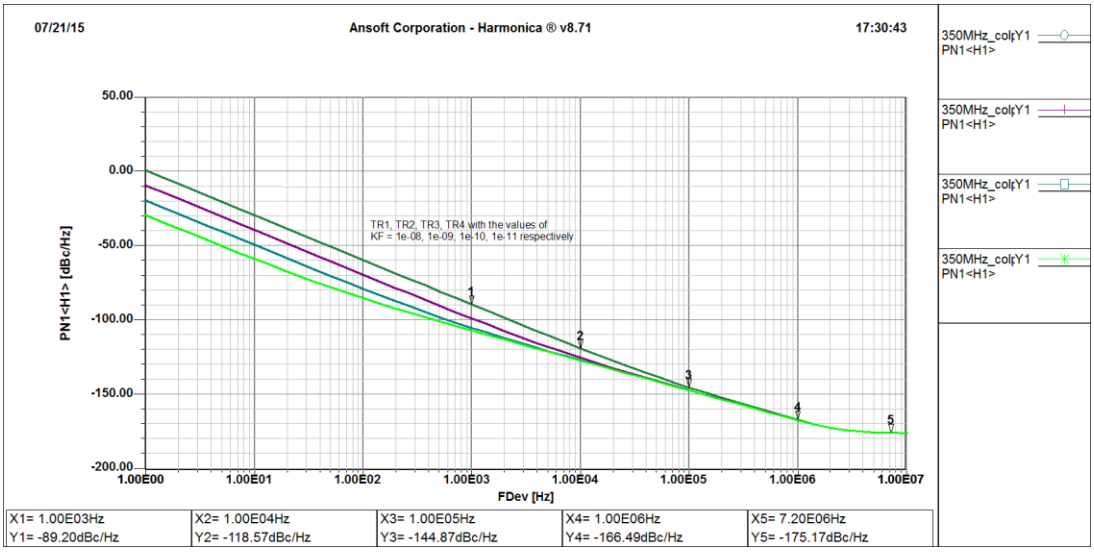


**Figure 19: Effect of KF factor on Phase Noise**

Changing the KF and AF factors, affects the phase noise as can be seen from the plots.

Y-intercept of the 1/f spectra increases proportionally to KF, which is in accordance with equation (34). The Y-intercept of the 1/f spectra decreases more rapidly with increase in AF. The following discussion of the tuning diodes results in a noise contribution similar to this flicker mechanism.

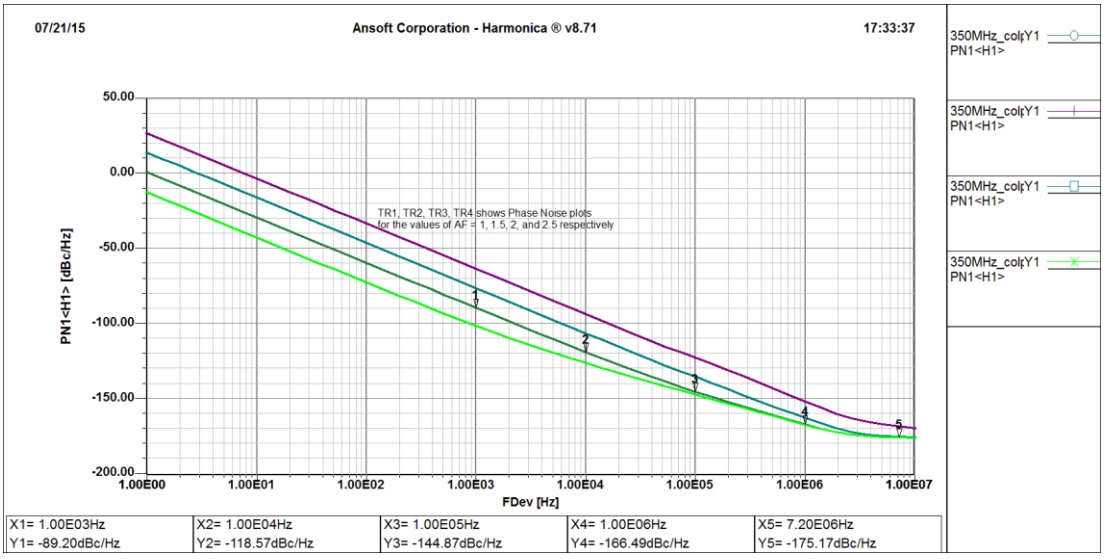


**Figure 20: Effect of AF factor on Phase Noise**

## AM-to-PM Conversion from tuning diodes

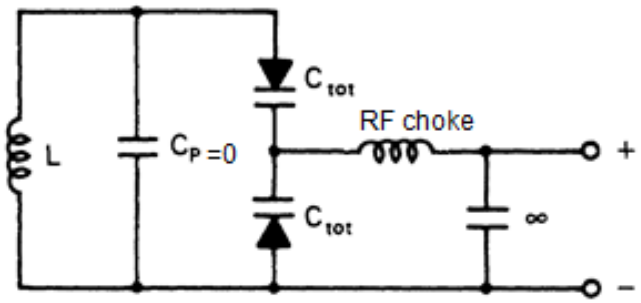


**Figure 21: Parallel tuned circuit with tuning diodes**

Figure 21 shows a parallel tuned circuit which is connected to the oscillator discussed above. The frequency change is obtained by applying a positive voltage to the + terminal. The parallel capacitor is replaced by the two tuning diodes. Here we will show the influence of the tuning diodes in the voltage-controlled oscillators, the resulting phase noise generated by tuning diodes is shown in Figure 22.

It is possible to define an equivalent noise $R_{aeq}$ that, inserted in Nyquist's Johnson noise equation,

$$V_n = \sqrt{4kT_o R\Delta f} \tag{69}$$

where $kT_o$=4.2 × $10^{-21}$ at about 300 K, $R$ is the equivalent noise resistor, and $\Delta f$ is the bandwidth, determines an open-circuit noise voltage across the tuning diode. Practical values of $R_{aeq}$ for carefully selected tuning diodes are in the vicinity of 200 Ω to 50 kΩ. If we now determine the noise voltage, $V_n = \sqrt{4 \times 4.2 \times 10^{-21} \times 10{,}000}$ the resulting voltage value is $1.296 \times 10^{-8}\ \mathrm{V}\sqrt{\mathrm{Hz}}$.

This noise voltage generated from the tuning diode is now multiplied with the VCO gain $K_o$, resulting in the rms frequency deviation

$$\left(\Delta f_{\mathrm{rms}}\right) = K_o \times \left(1.296 \times 10^{-8}\ \mathrm{V}\right) \text{ in 1-Hz bandwidth} \tag{70}$$

To translate this into an equivalent peak phase deviation,

$$\theta_d = \frac{K_o\sqrt{2}}{f_m}\left(1.296 \times 10^{-8}\right) \text{ rad in 1-Hz bandwidth} \tag{71}$$

or for a typical oscillator gain of 100 kHz/V,

$$\theta_d = \frac{0.00183}{f_m} \text{ rad in 1-Hz bandwidth} \tag{72}$$

For $f_m$ = 25 kHz (typical spacing for adjacent-channel measurements for FM mobile radios), the $\theta_c$ = 7.32 × $10^{-8}$. This can be converted now into the SSB signal-to-noise ratio:

$$\mathcal{L}(f_m) = 20\log_{10}\frac{\theta_c}{2} = -149\ \mathrm{dBc/Hz} \tag{73}$$

For the typical oscillator gain of 10 MHz/V found in wireless applications, the resulting phase noise will be 20 dB worse [10 log (10 MHz ÷ 100 kHz)]. However, the best tuning diodes, like the BB104, have an $R_n$ of 200 Ω instead of 10 kΩ, which again changes the picture. Therefore, with $kT_o$ = 4.2 × $10^{-21}$ the resulting noise voltage will be

$$V_n = \sqrt{4 \times 4.2 \times 10^{-21} \times 200} = 1.833 \times 10^{-9}\ \mathrm{V}\sqrt{\mathrm{Hz}} \tag{74}$$

From (72), the equivalent peak phase deviation for a gain of 10 MHz/V in a 1-Hz bandwidth is then

$$\theta_d = \frac{1\times10^7\sqrt{2}}{f_m}\left(1.833\times10^{-9}\right) \text{ rad} \tag{75}$$

or

$$\theta_d = \frac{0.026}{f_m} \text{ rad in 1 - Hz bandwidth} \tag{76}$$

With $f_m$ = 25 kHz, $\theta_c = 1.04 \times 10^{-6}$. Expressing this as phase noise:

$$\mathcal{L}(f_m) = 20\log_{10}\frac{\theta_c}{2} = -126 \text{ dBc/Hz} \tag{77}$$

Figure 22 shows the influence of the tuning diode on the phase noise. For the purpose of discussion, the equivalent noise resistance is assumed 1kΩ, and 3 sensitivity curves are shown. For a tuning sensitivity of more than 100 kHz/V the varactor noise dominates. As the tuning sensitivity increases the influence of the oscillator noise itself disappears.

**Summary:**

With a systematic approach to the Colpitts oscillator this paper provides information for an optimized design and the resulting phase noise. Starting with the explanation about the Colpitts oscillator, invented in 1918, we have discussed a linear analysis based on Y-parameters, followed by S-parameter approach, which is applicable to practically all oscillators and then move into the important time-domain analysis. This allows a very reliable design, where the simulated, calculated and the measured results agree well. This detailed analysis gives a thorough insight into the design approach and results of a Colpitts oscillator. Finally the noise contribution of the tuning diodes is added. The interested reader, having access to CAD tools can run some "experiments" by varying the component values.

At this point we would also like to thank our reviewers for their valuable suggestions to optimize this paper.

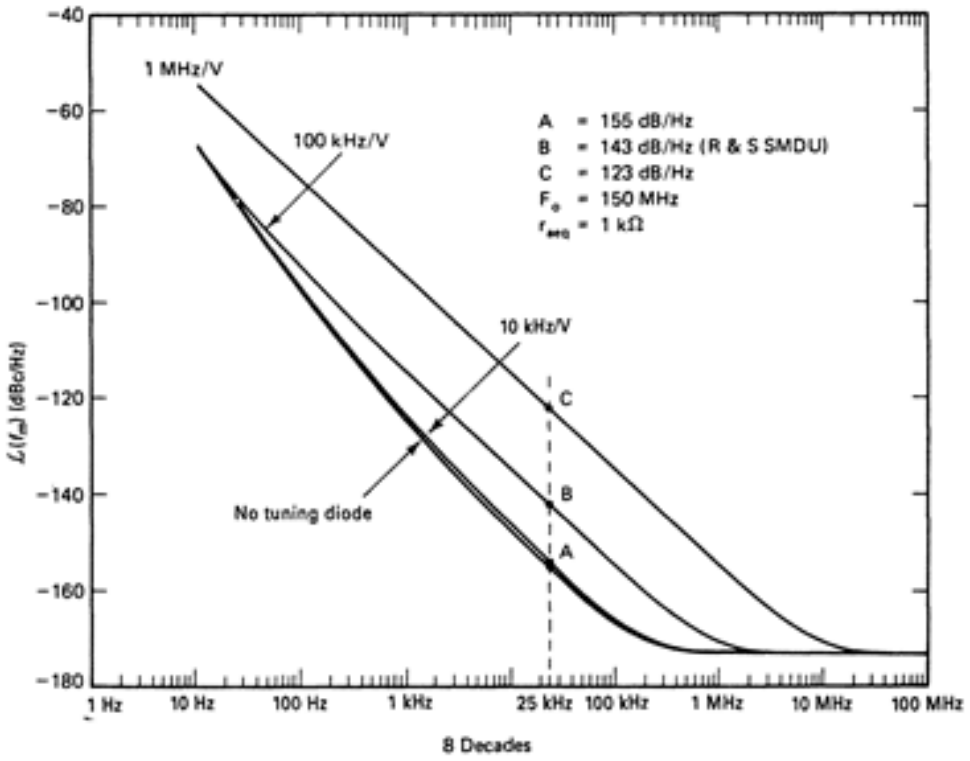


**Figure 22: Influence of tuning diode on phase noise**

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