Quartz Crystal Oscillator Design

Introduction :

In many applications, electromechanical resonators, such as quartz crystals are used as frequency selective element. Quartz crystals have the property of piezoelectricity. Devices with piezoelectric effect undergo mechanical deformation with the influence of applied electric charge and vice-a-versa. Due to this property, they are primarily used to form a resonator in oscillator circuit. Most of the communication systems rely on the quartz crystal as reference oscillator for synthesis of the harmonic signal required for their operation. The crystal (reference) oscillators are design for a stable reference frequency oscillator of 10MHz or 5Mhz and recently the higher frequency 100MHz or 120MHz for frequency synthesizers. Many of them are synchronized against Rubidium or Cesium standards.

The modern communication systems are particularly susceptible to reference oscillator phase noise because the process of frequency multiplication increases the power in the sidebands by the square of the multiplication factors. The phase noise of these sources limits the noise floor and interference susceptibility that affects directly the system performance, like bit error rate in point to point radios, range and load capability of telephone networks, reliability of navigation systems, detection ability of radars etc. Therefore designing low phase noise crystal oscillator is challenging for a given cost, size and power-consumption.

Any oscillator including such with extremely high Q transfers DC energy to RF energy, with some key parameter being most important.

These are: Extremely low phase noise
Short term and long term stability (aging)
Specified RF power output and low harmonic content
Pushing and pulling
DC power supply and DC tuning voltage to name a few

Here is a typical Data sheet from one of the world's best oscillator manufacturer

Wenzel Associates, Inc.
"Quietly the Best"

Crystal Oscillators > 4 to 30 MHz > HF Ultra Low Noise OCXO

Features:

- Lowest Phase Noise Available
- Good Frequency Stability over Temperature
- Internal Voltage Regulator
- Very Low Aging Rate

Applications:

- Radar Systems
- Reference for Phase Noise Measurements
- Synthesizers

Typical Specifications:						
Frequency *(Specify)*		4 to 30 MHz				
Frequency		5		10		MHz
Output Level		+13				dBm
Aging		$\pm 1 \times 10^{-9}$ to $\pm 1 \times 10^{-10}$ / day after 30 days				
Phase Noise						
	10 Hz	-115	-120	-130	-132	dBc/Hz
	100 Hz	-145	-150	-158	-162	dBc/Hz
	1 kHz	-165	-170	-172	-172	dBc/Hz
	10 kHz	-176	-176	-172	-175	dBc/Hz
Temperature Stability *(Specify)*		$\pm 5 \times 10^{-8}$ to $\pm 2 \times 10^{-8}$				
Range A	0 to +50C					
Range B	0 to +65C					
Range C	0 to +70C					
Range D	-20 to +70C					
Range E	-40 to +70C					
Range F	-55 to +85C					
Electrical Tuning Range *(Specify)*		$\pm 2 \times 10^{-7}$ to $\pm 2 \times 10^{-6}$				
Tuning A	0 to +10 VDC					
Tuning B	±5 VDC					
Supply Voltage *(Specify)*		+12 or +15				VDC
Warm-up Power		5 for 5 minutes				Watts
Total Power *typical*		2.5 @ 25°C				Watts
Crystal Type		SC				
Dimensions		44.4 x 74.7 x 25.4 1.75 x 2.94 x 1				mm inches
Connectors		SMA on side and solder pins on base				

These high performance oscillator are typically available in 5 MHz, 10 MHz, 80 MHz, 100 MHz and up to 120 MHz The higher frequency value oscillators are mostly voltage controlled crystal oscillators (VCXOs), but even the 5 MHz versions have a very small tuning range synchronize them with atomic frequency standards

Visiting Crystal Theory:

In many applications, electromechanical resonators, such as quartz crystals are used as frequency selective element. Quartz crystals have the property of piezoelectricity. Devices with piezoelectric effect undergo mechanical deformation with the influence of applied electric charge and vice-a-versa. Due to this property, they are primarily used to form a resonator in oscillator circuit. The commonly found resonators in the microwave/RF designs other than crystal resonators are LC, Microstrip, Ceramic, Dielectric, and YIG. Though each resonator has its advantage and disadvantage for use in particular application, generally the crystal oscillators are preferred as an option to design a stable reference frequency oscillator of 10MHz or 5Mhz and recently the higher frequency 100MHz or 120MHz for frequency synthesizers. These quartz crystal resonators suffer from multi-mode resonances and cross-talk due to large holding capacitance.

Figure (1) shows the typical impedance characteristics of electromechanical crystal resonator, which vibrates due to piezoelectric effect and exhibits multimode resonances.

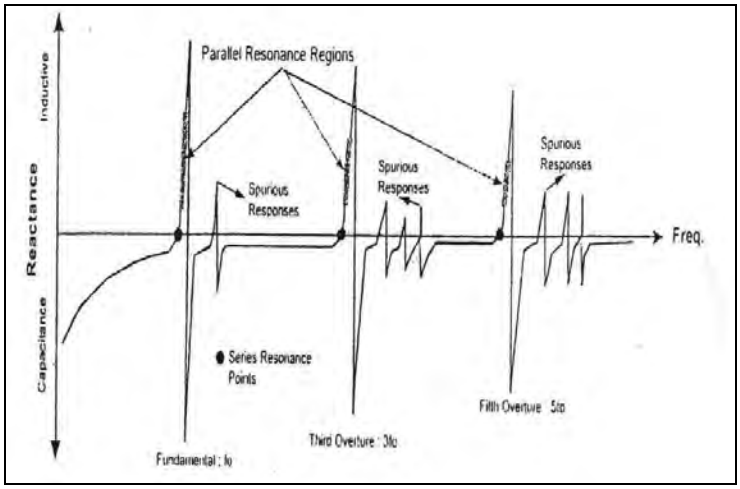


Figure 1: Fundamental and the overtone resonance [3]

Crystal Resonator: The crystal resonator is obtained from the abundant natural resource of quartz. The quartz stone gets cut into thin slices called “blank”, which are coated with metallic films that form the leads for exciting the crystal. The quartz is cut in various ways either in single rotation or double rotation, which results in significant change in the operating parameters mainly the operational frequency stability. This is more elaborated in the [1], [2] and [3] references. The commonly used blanks are formed from AT cut and SC cut quartz. The cut of the quartz also results in additional resonances, specifically in SC and IT cut crystals. These additional resonances termed as b-mode are located at approximately 10% higher in frequency from the desired c-mode. Apart from b-mode we also get the

a-mode resonance at a $\frac{188}{100}$ times the c-mode. The accompanying figure (2), explains position of modes for an SC cut crystal resonator.

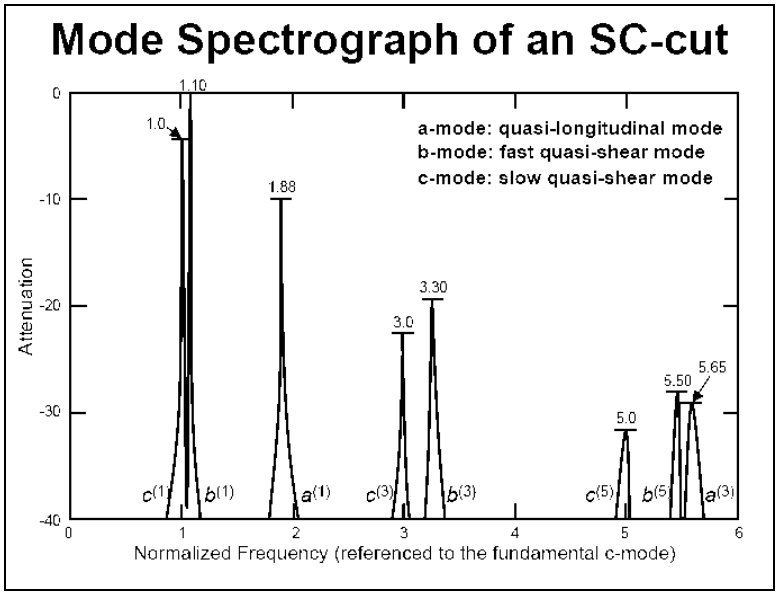


Figure 2: Modes for an SC cut Crystal resonator [2]

B-mode: The b-mode has a linear temperature characteristics and can be used as a sensitive thermometer of the resonator temperature. This effect has been used to design extremely stable microcomputer-compensated oscillators, where the frequency of b-mode ia used to compensate the fundamental mode and oscillations are present on both modes at all times.However more typically its required the crystal is operated only on a single mode. A resonant circuit must then be employed to trap out the b-mode and force the oscillations to occur on the desired mode at all times. This is b-mode trapping. Depending upon the circuit configuration, several different methods can be employed. This can be accomplished in Colpitts and Pierce oscillator by forcing one of the capcitive element to be inductive at the frequency of unwanted mode. As shown below the inductors L2 and C2 are series resonant at freuqency just below the b-mode. This means that they appear inductive at the b-mode frequency, thus they serve as b-mode trap. The net impedance of this circuit is shown below:

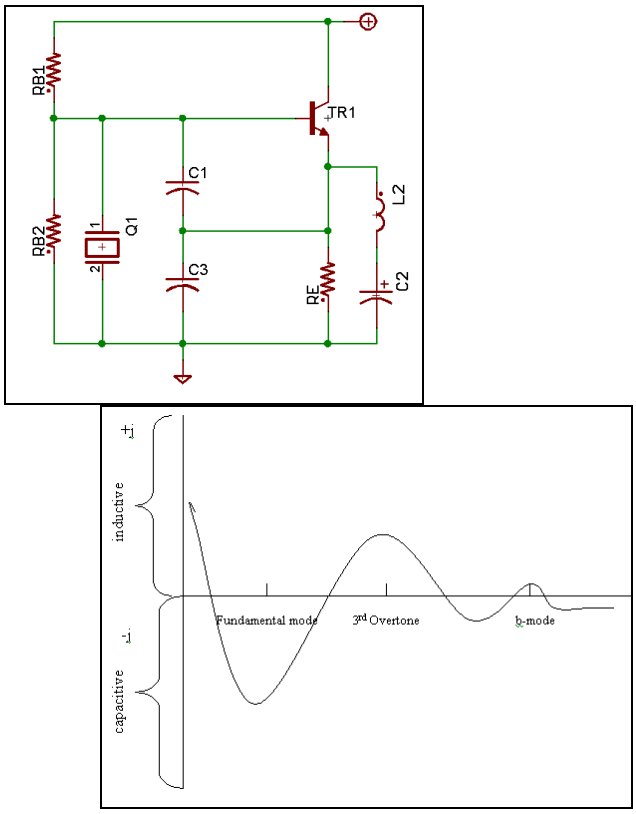


Figure 3: b-mode trap schematic and the net impedance for b-mode trap.

It can be very convenient to measure thermal performance of an oven using the b-mode. By returning the resonant circuit to force oscillations to occur on the b-mode, the linear frequency verses temperature characteristics can provide a means to precisely measureing the performance of the thermal enclosure. To accomplish this, the frequency variations caused by temperature changes of the b-mode are first measured with the oven off. This step provides a measn of characterizing the frequency-temperature characteristics of the b-mode. Next, the frequency change caused by external temperature variations are computed from this. Of course, the trap can then be retuned to set the oscillation back to the desired mode.

The equivalent circuit of a crystal at resonance can be shown as a series combination of RLC in parallel with a holding capacitor. The package capacitances and lead inductance are generally ignored till the VHF frequencies. The equivalent circuit for crystal shows two resonances, one due to the series branch alone and the other with the inductor L in combination with the effective capacitance of C0 and C1…Cn. These resonances are called the series resonant frequency and the anti-resonant frequency of the crystal and computed as,

$$fs = \frac{1}{2\pi\sqrt{L1\,C1}} \quad \text{and} \quad fp = \frac{1}{2\pi\sqrt{L1\left(\frac{C1\;C0}{C1+C0}\right)}}$$

where, *'fs'* is series resonant frequency and *'fp'* is the anti-resonant frequency [1].

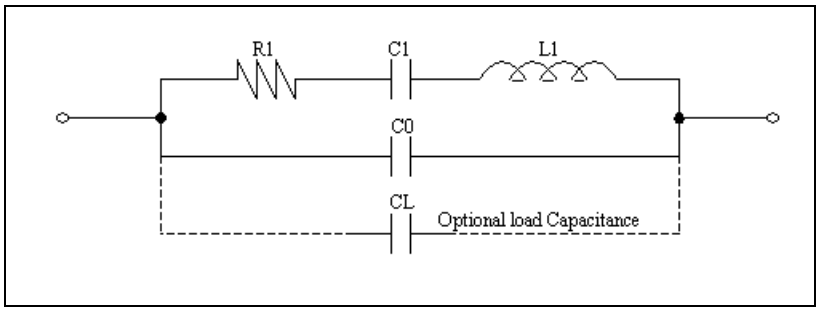


Figure 4: Equivalent Circuit of a crystal resonator with the optional CL capacitor [1]

When an oscillator presents some amount of load capacitance to a crystal, the crystal is said to be *parallel resonant*, and a value of load capacitance, CL, must be specified. If the circuit does not exhibit capacitive loading, the crystal is said to be *series-resonant*, and no value of load capacitance is specified. It is important to note that when a capacitor is placed in series with a crystal, the new series frequency is displaced slightly to a higher frequency than the original series resonance. Conversely, when the capacitor is placed in parallel with the resonator, the new parallel resonant frequency is displaced slightly to a lower frequency. This phenomenon has caused a great deal of perplexity between the terms series and parallel resonance. Series mode resonance of the crystal is represented by a small resistance in series with a resonant reactance, whereas, in parallel mode by a large resistor in parallel to a resonant susceptance. The series (f_i) and parallel resonance (f_p) are described by the impedance function,

$$Z(s) = \frac{1}{sC_0 + \dfrac{1}{1/sC_i + sL_i + R_i}} = \frac{s^2 + sR_i/L_i + 1/L_iC_i}{sC_0[s^2 + sR_i/L_i + (C_0 + C_i)/L_iC_iC_0]}$$

The further evaluation from the imaginary part of the zeroes

$$s_{z1,2} = -\frac{\omega_0}{2Q} \pm j\omega_0\sqrt{1 - \frac{1}{4Q^2}} \quad \approx \quad -\frac{\omega_0}{2Q} \pm j\omega_0, \quad for \quad Q >> 1$$

and poles as below,

$$s_{p1,2} = -\frac{\omega_0}{2Q} \pm j\omega_0\sqrt{1 + \frac{C_i}{C_0} - \frac{1}{4Q^2}} \approx -\frac{\omega_0}{2Q} \pm j\omega_0\left(1 + \frac{C_i}{2C_0}\right)$$

$$\omega_i = \frac{1}{\sqrt{L_iC_i}} \Rightarrow f_s(series) = \frac{1}{2\pi\sqrt{L_iC_i}}$$

$$\omega_p \approx \omega_0\left(1 + \frac{C_i}{2C_0}\right)\Big|_{C_0 >> C_i} \Rightarrow f_p(parallel) \approx \frac{1}{2\pi\sqrt{L_iC_i}}\left(1 + \frac{C_i}{2C_0}\right)\Big|_{C_0 > C_i}$$

$$M = \frac{2Q(\omega_p - \omega_0)}{\omega_0} = \frac{2Q(f_p - f_0)}{f_0}$$

gives us M, mode separation (f_p - f_0) equation. The degree to which an oscillator generates a constant frequency f_i throughout a specified period of time is defined as the frequency stability of the signal source.

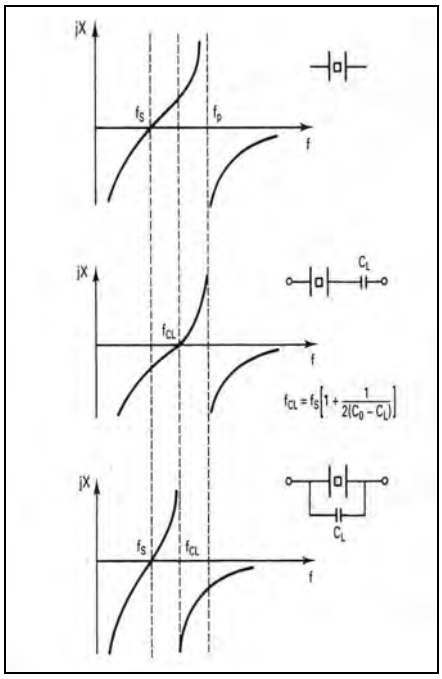


Figure 5: Crystal resonance with and with out the effects of load capacitance, *CL*.

Crystal does not produce harmonics and the overtone response of crystal is not harmonics of fundamental. For designing the high performance crystal oscillator, the oscillator circuit topology determines the crystal configuration, like use of fundamental, overtone, parallel and the series configuration. In other words, the oscillator circuit topology forces the crystal resonator into either the fundamental (lowest major resonant response), overtone (major responses other than fundamental), parallel (one of the inductive regions of the crystal's reactance curve) or series mode (one of the resistive points on the crystal's reactance curve) of operation.

For overtones the equivalent circuit of crystal gets an additional branch in parallel with a combination of RLC (not shown in above diagram). The values of R, L and C in the overtone branch can be computed by scaling the values of R, L and C in the fundamental resonant branch. If '*f*1' is the fundamental frequency then the nth overtone frequency should be computed as,

$$fn = n * f1 = \frac{1}{2\pi\sqrt{Ln\ Cn}} = \frac{n}{2\pi\sqrt{L1\ C1}} = \frac{1}{2\pi\sqrt{L1\frac{C1}{n^2}}}$$

$$\Rightarrow Ln = L1$$

$$\Rightarrow Cn = \frac{C1}{n^2} \quad where, n\ is\ 3,5,7\ etc\ldots\ overtone\ number$$

Wide pull Voltage controlled crystal oscillator (VCXO) typically utilizes fundamental crystals with large motional capacitance C1. Overtone operation is

precluded if wide tuning range is desired. Also the resistor for the overtone branch gets scaled as $Rn = R1 * n^2$, which implies that the negative resistance required to get oscillations on overtone is much larger than the value for fundamental mode. The fundamental frequency (lowest-mode) response is the most active due to lowest value of Rn. If a large negative resistance is provided for the fundamental resonance, it could result in exciting an overtone mode also. For designing high frequency crystal oscillators, generally the crystal is excited on its overtone mode and care should be taken to suppress the unwanted fundamental resonance in such cases.

Apart from the spurious resonances, the cut of the quartz resonator changes the angle of the crystalline orientation that leads to change in crystals behavior over the temperature. The temperature behavior is modeled by a third order polynomial of the form $\frac{\Delta f}{f} = a(t - T0) + b(t - T0)^2 + c(t - T0)^3$, where T0 is the inflection temperature [1], at which the change in frequency is minimum.

General examples of frequency changes over temperature, generally referred to as FT behavior observed in the range of -50^0c to $+125^0$c are shown in the figure (6) and figure (7). The FT behavior shows the crystals upper and lower turning points along with the inflection angle. To minimize the frequency changes resulting from temperature the oven of the OCXO is adjusted to the turning point of the crystal. Note for an AT cut crystal of 9 minutes, shows frequency change of about ±30ppm and inflection angle at 27^0c while an SC cut crystal of 9 minutes, shows the inflection angle around $+100^0$c with the changes in frequency from -225ppm to +50ppm.

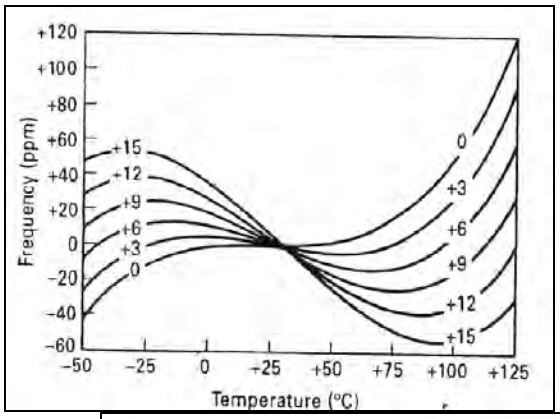


Figure 6: FT for AT cut resonators

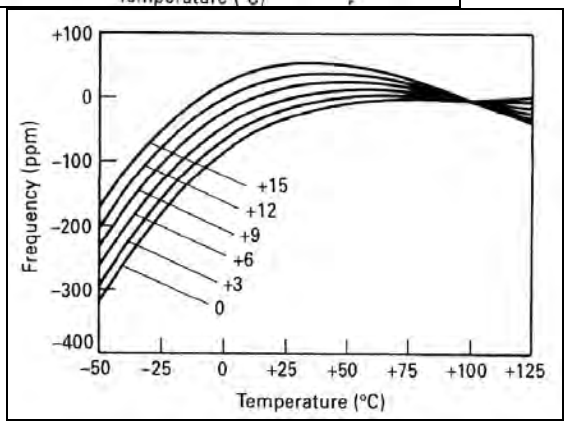


Figure 7: FT for SC cut resonators

In an SC cut and IT cut resonators the change in frequency is more towards the cold end but tend to flatten out as the temperature approaches the inflation angle as shown in figure (8). This makes them very suitable for Oven controlled oscillators where the temperature of the oven is set to the turn temperature. The AT cut on other hand has inflection angle around 27^0c, and that makes it suitable for TCXO application.

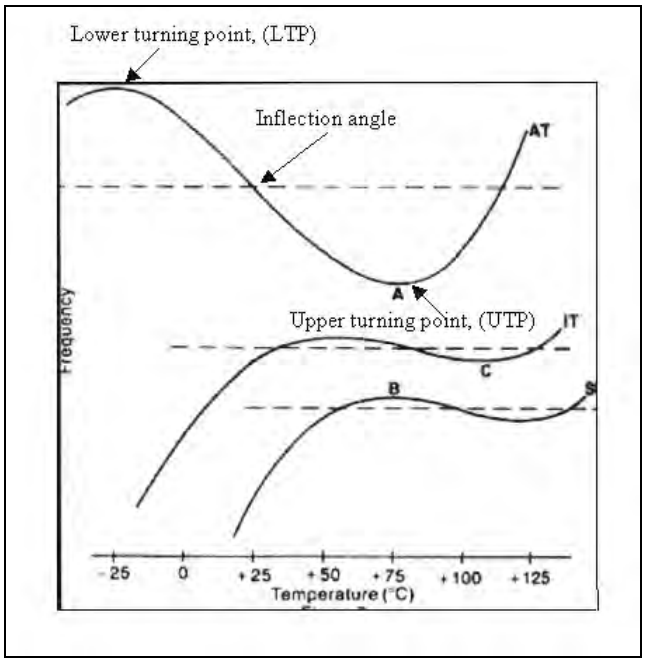


Figure 8: FT for AT cut, SC cut, IT cut resonators showing UTP, LTP and inflection angle.

The frequency variations in AT cut resonator are dependent on temperature and the thermal gradient of temperature across the crystals surface, where as the SC cut is immune to the thermal gradients. Since SC cut is nearly insensitive to the thermal gradients that invariably occur during oven warm-up, it is expected that SC cut resonators will give much faster warm-up in ovenized oscillators. The packaging and the control circuitry play a critical role in warm-up time of ovenized crystal oscillator.

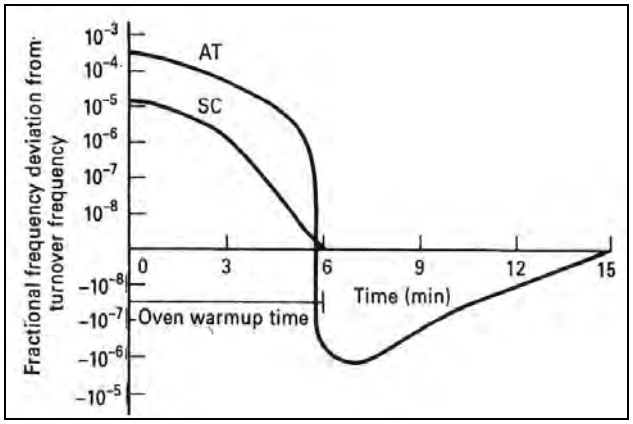


Figure 9: Typical warm-up for AT and SC cut oven oscillators

Another property of crystal is aging. This is strongly affected by cleanliness of the resonator and enclosure. A thin resonator is more affected of low aging by thin film of contamination than a thicker resonator. Also stress relaxation of the mount

structure and electrodes, excessive crystal drive power and out-gassing of materials in crystal support structure and electrodes contribute towards aging.

The commonly used crystal oscillators based on the compensation techniques are:

OCXO (Oven Controlled Crystal Oscillator): In OCXO the crystal and other temperature sensitive components are placed in a stable oven, which is adjusted to the temperature where the crystal's FT characteristics has zero slope. This is achieved by setting the oven temperature to either the LTP (lower temp) or UTP (upper temp), where the FT variations of the crystals are minimum. OCXOs can provide a >1000X improvement over the crystal's f vs. T variation. This can help in achieving stringent frequency stability as compared to a basic crystal oscillator design. These normally involve SC cut crystals.

TCXO (Temperature Compensated Crystal Oscillator): The temperature stability of the basic oscillator can be improved by incorporating the inverse temperature characteristics to nullify the FT of crystals. This type of crystal oscillators prefers to use AT cut crystals. Based on the circuit involved in its design TCXOs are categorized into two different types. One that employs a microcontroller is DTCXO, Digital TCXO and the other circuit uses thermistor network to control the temperature circuit termed just as TCXO or ATCXO, Analog TCXO. The technique employs a thermistor network and varactor in series with the crystal. Over the temperature the thermistor network would generate a voltage, which will be the inverse characteristics of the crystal. This voltage is applied across the varactor, which changes the capacitance in series with the crystal to bring it back to desired frequency. The stability requirements of most TCXOs dictate compensation by means of a multiple thermistor network with several interdependent variable components thus making the solution of simultaneous equations by computer the only feasible approach to temperature compensation. When the temperature compensation has stringent requirements then instead of the thermistor, it is preferred to use an ASIC or microcontroller based design, in which the microcontroller is programmed to generate the inverse FT response.

VCXO (Voltage Controlled Crystal Oscillator): These oscillators include a varactor diode in the circuitry, which allows frequency to be tuned to slightly different values. It can further be either temperature compensated (called TCVCXO) or Oven controlled (called OCVCXO) for better performance.

In general the floor of the TCXO's can be an almost as good as high stability ovenized oscillator, but the close-in phase noise and short-term stability are very poor relative to oven. This is because of the need to pull the oscillator frequency of a TCXO mandates a low resonator Q relative to an ovenized oscillator. The digital compensation of TCXO is constrained to not more than ±0.05ppm by the limitations of effects such as hysteresis in the frequency/temperature characteristics of the crystal and the adjustments required compensating for aging.

In broad view there should be 5 specifications for a crystal oscillator as follows:

Define Type of Oscillator	Attach Reference documents	Mention following Electrical Properties	Environmental Properties	Quality Assurance
TCXO VCXO OCXO etc..	Tests to be performed Testing methods Miltary Specifications if any etc..	Nominal Frequency ± Tolerance (ppm/0c) Output power and type of output Supply voltage ± supply tolerance Supply current ± current tolerance Tunning Range Warmup conditions Supply sensitivity Load sensitivity Phase noise and/or Allan variance Aging (per day, per year etc..) Radiation, accelaration sensitivity Magnetic field sensitivity	Temperature range operation storage Vibration Shock	any other test required that add upto the cost of unit Special markings etc..

A modern design approach for crystal oscillators using different circuits :

Certain requirements were set-forth to be fulfilled from this design. The main objective was to design a 10MHz crystal oscillator , one example with low phase noise, an output power of 10dBm with a voltage supply of 10 to 12 V and the load resistor is assumed to be 50 ohms.

For the first example the operational frequency is 10MHz, and the semi-isolated colpitts configuration is selected for the design. The Colpitts configuration is generally good for crystal oscillator design and good performance up to 50MHz and is also very simple to design. With the semi-isolated configuration, the output is taken from the collector that has higher ratio of output power level to crystal power. Changing the biasing component values but still maintaining the same output current we will be able to change the performance of phase noise [5, pp230].

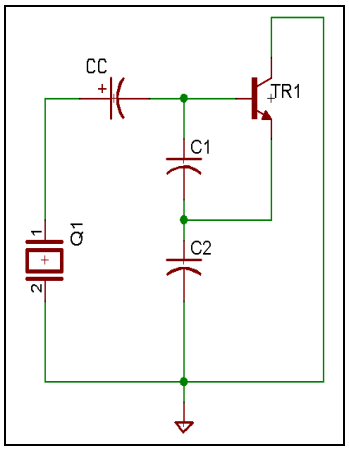


Figure 1: Basic Colpitts crystal oscillator

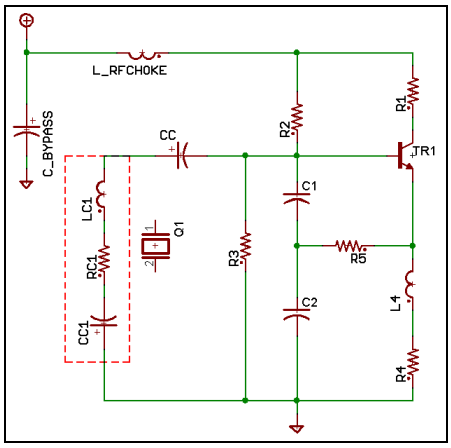


Figure 2: Colpitts oscillator—Crystal replaced with its equivalent schematic

To proceed through the design procedures and to calculate the values of each component, replace the crystal with its LC equivalent circuit and Q specified in the schematic as shown in figure 2. The first step in the design process involved calculating the operating point for fixed normalized drive of x=20 (table 6-1 from reference [5]). The output voltage $V_{out}(\omega_0)$ and current $I_{out}(\omega_0)$ at the fundamental frequency based on the output power requirements can be computed with following equation from ref. [5].

$$V_{out}(\omega_0) = \sqrt{P_{out}(\omega_0) * 2R_L} = \sqrt{0.01 * 2 * 50} = 1V$$

$$I_{out}(\omega_0) = \frac{V_{out}(\omega_0)}{50} = 20\,mA$$

$$where,\ output\ Power\ \left(P_{out}(\omega_0)\right) = 10dBm = 10mW$$

The DC operating point is calculated based on the normalized drive level x=20. The expression for the emitter dc current, $I_E(\omega_0) = I_{out}(\omega_0)$, can be found in terms of the Bessel function with respect to the drive level as (Ref. [5]).

$$I_E(\omega_0) = 2I_{DC}\left[\frac{I_1(x)}{I_0(x)}\right] \Rightarrow I_{DC} = 10.26mA$$

The NEC transistor BFP193 was selected and biased as shown in figure 3. The resistor values were determined such that they satisfy our requirements of 10V supply and 10mA current.

$$Assume \quad Vce = 4.2\ v$$

$$\beta = 100$$

$$Ve = 4.7\ v$$

$$Ie = Ic + Ib$$

$$Ib = \frac{Ic}{\beta} = \frac{10\ mA}{100} = 0.1\ mA$$

$$\therefore Ie = 10.1\ mA$$

$$Ve = Ie * R4$$

$$\Rightarrow R4 = 465.3\ \Omega \approx 470\ \Omega \quad std$$

$$R1 = \frac{Vcc - (Ve + Vce)}{Ic} = 100\ \Omega \quad std$$

$$Vb = 5.4\ v = \frac{Vcc * R3}{R3 + R2}$$

$$\Rightarrow \quad R3 = 15\ K\Omega \quad if \ \ R2 = 10\ K\Omega$$

The circuit with calculated values was simulated in Ansoft designer for DC analysis and the currents and voltage verified. The third step involves calculating the large-signal transconductance Y21 parameter from the table 6-1 and 6-2 in reference [5].

$$Y_{21}\big|_{lg} = G_m(x) = \frac{qI_{DC}}{kTx}\left[\frac{2I_1(x)}{I_0(x)}\right]_{f=fundamental}$$

$$\left[Y_{21}\right]_{\omega=\omega_0} = \left[\frac{1.949 I_{E-DC}}{520mV}\right] = 50.83mS$$

Here the term $Y_{21}\big|_{lg}$ is the large signal transconductance.

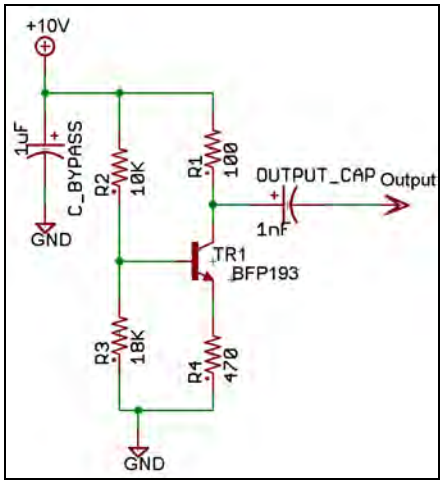


Figure 3: Fixed biasing for bipolar transistor BFP193

The transformation factor *n* is calculated based on the quadratic equation and the large-signal transconductance parameter of transistor BFP193 [5,Ch 6]. The value of n is selected from the set of n1 and n2, both inclusive, for a given drive-level, x=20.

$$n^2(G2+G3)-n(2G3+Y21\alpha)+(G1+G3+Y21)=0$$
$$\Rightarrow n1=17.2581 \quad and \quad n2=1.0251$$
$$Let \quad n=2$$
$$C1=58.9\,pF \quad and \quad C2=58.9\,pF$$
$$Cc=33\,pF$$
$$Ceff=\frac{Cc*C1*C2}{C2*Cc+C1*Cc+C1*C2}=15.576\,pF$$
$$Leff=86.878uH$$

The values calculated are for the circuit in figure 2. C1 and C2 are the capacitors in capacitive feedback network, while Cc is the coupling capacitor. The *Leff* , is the effective inductance required to form oscillations. The above circuit oscillates with a lumped inductor of value *Leff* and the phase noise is not so good due to the assumption of less Q for the resonator while, the output frequency of the circuit as revealed by the non-linear analysis from serenade program is 9.242MHz.This exercise was done to harmonize that a Colpitts oscillator needed an inductor or inductive resonator with the capacitive divider feedback to form oscillations. The above design values give a reliable preparatory point to further optimizing the design. The values of Q (defined by Rc1), Lc1 (Lc1= *Leff* as initial design step) and Cc1 (initial value computed such that $XLc1+\frac{1}{XCc1}=0$) in figure (2) are then scaled and tuned to match the crystal parameters to be used. In general the inductance of the crystal is in few Henrys and the capacitance is in few Femto-Farads while the Q of the crystal is a few millions.

We have assumed the value of transformation factor, $n=2$, which require that the design have feedback capacitors of 59pF, this can be further optimized to get the minimum phase noise. The value of n, transformation factor is varied for optimum phase noise and output power and is generally computed from the derivative of the phase noise equation, as shown in Ref. [5], and written the following form [5, pp181],

$$\frac{\partial}{\partial y}\left\{\left[k0+\left(\frac{k^3k1\left[\frac{Y_{21}|_{lg}}{Y_{11}|_{lg}}\right]^2 y^{2P}}{Y_{21}|_{lg}{}^3\, y^{3Q}}\right)*\left(\frac{1}{y^2+k}\right)\right]*\left[\frac{(1+y)^2}{y^2}\right]\right\}_{y=m}=0$$

where, $Y_{21}\big|_{lg}$ is the large signal transconductance and $Y_{11}\big|_{lg}$ is the large signal admittance.

$$k0 = \frac{\kappa TR}{\omega^2 \omega_0^2 L^2 V_{CE}^2 C_2^2}$$

$$k1 = \frac{qI_c gm^2 + \left(K_f \frac{I_b^{A_f}}{\omega} \right) gm^2}{\omega^2 \omega_0^2 L^2 V_{CE}^2}$$

$$k2 = \omega_0^4 \beta^2$$

$$k3 = gm^2 \omega_0^2$$

$$k = \frac{k3}{k2C_2^2} \Rightarrow C_2^2 = \frac{k3}{kk2}$$

$$y = \frac{C_1}{C_2}$$

Here, K_f is the flicker noise coefficient, *AF* is the flicker noise exponent, *R* is the equivalent loss resistance of the tuned resonator circuit, I_c is the RF collector current, I_b is the RF base current, V_{CE} is the RF collector voltage, C_1, C_2 is the feedback capacitor, *P* and *Q* are the drive level dependent constant across base-emitter of the device. From curve-fitting attempts, the following values for *P* and *Q* were determined (*P* =1.3 to 1.6; *Q* =1 to 1.1).

The simulation for different values of n and the C1, C2 computed for that value of n shows the following phase noise and output power results. A lower value of n can be opted at the cost of increased harmonic outputs.

n	C1 (pF)	C2 (pF)	dBc/Hz@ 10Hz	dBc/Hz@ 100Hz	dBc/Hz@ 1KHz	dBc/Hz@ 10KHz	dBc/Hz@ 100KHz
1.10	33	330	-117.5	-128.0	-138.1	-148.0	-157.8
1.20	36	180	-120.9	-131.0	-141.0	-150.9	-160.5
1.30	39	124	-116.7	128.9	-138.9	-148.8	-158.5
1.35	39	110	-114.3	-128.5	-138.6	-148.5	-158.2
1.40	42	100	-112.0	-127.6	-137.5	-147.7	-157.2
1.50	47	82	-108.2	-126.7	-136.5	-146.5	-156.2
2.00	59	59	-100.8	-127.6	-137.0	-147.0	-156.6
2.50	75	47	-95.4	-125.4	-140.0	-150.0	-159.8
3.00	82	47	-97.9	-127.8	-139.0	-149.4	-159.0
4.00	110	39	-94.6	-124.6	-141.8	-151.7	-160.9

The design is almost complete. We may need some additional filtering components to filter out the harmonic contents for the circuit. The harmonic contents are function of drive level. As the drive level increase the harmonic contents also increase and additional filtering is required for the proper suppression of harmonic contents. We can now compute the noise factor and the phase noise of the system from all the components values. We use the following equation to compute the noise factor for the oscillator from ref.[5 pp. 133].

$$F = 1 + \frac{Y_{21}|_{lg} C_2 C_C}{(C_1 + C_2) C_1} \left[r_b + \frac{1}{2 r_e} \left[r_b + \frac{(C_1 + C_2) C_1}{Y_{21}|_{lg} C_2 C_C} \right]^2 \left[\frac{1}{\beta|_{lg}} + \frac{f_0^2}{f_T^2} \right] + \frac{r_e}{2} \right]$$

where, r_b is the base resistance, $r_b = 7.2326\Omega$ while r_e is the emitter resistance of the transistor $r_e = 1.0075\Omega$ and f_T is the transition frequency for the transistor $f_T = 5GHz$. The large signal current gain is given as $\beta|_{lg} = \frac{Y_{21}|_{lg}}{Y_{11}|_{lg}} \left(\frac{C_1}{C_2} \right)^P$.

The mathematically computed value for noise factor is 2.0016 and the noise figure for the oscillator given as $noiseFigure = 10 * \log 10(F)$ was computed to be 3.01385dB for transformation factor, n=2.

The final step in the approach is to calculate the phase noise from the following equation of ref [5, pp.131 equation; 7-26]

$$L(f_m) = 10 \log \left\{ \left[1 + \frac{f_0^2}{(2 f_m Q_L)^2} \right] \left(1 + \frac{f_c}{f_m} \right) \frac{FkT}{2 P_{sav}} + \frac{2 kTRK_0^2}{f_m^2} \right\}$$

where, Q_L is the loaded Q factor of the oscillator, F is the noise factor, kT is Boltzman's constant, R is the equivalent loss resistance of the tuned resonator circuit or equivalent noise resistance of tuning diode (typically 50Ω -10kΩ), and P_{sav} is the average power at oscillator output, K_o = voltage gain. The phase noise of the system has been determined theoretically and agrees with simulated response from Ansoft Serenade [6]. The figure (4) and figure (5) below shows the phase noise and the output power plot from the Serenade program.

f_m	1Hz	10Hz	100Hz	1000Hz	10KHz	1
Phase noise	-66.85	-96.18	-121.44	-137.68	-147.65	-

The calculated phase noise (shown in the table) for offset frequency f_m from the carrier frequency f_0 agreed closely to the simulated values (shown in figure 4).

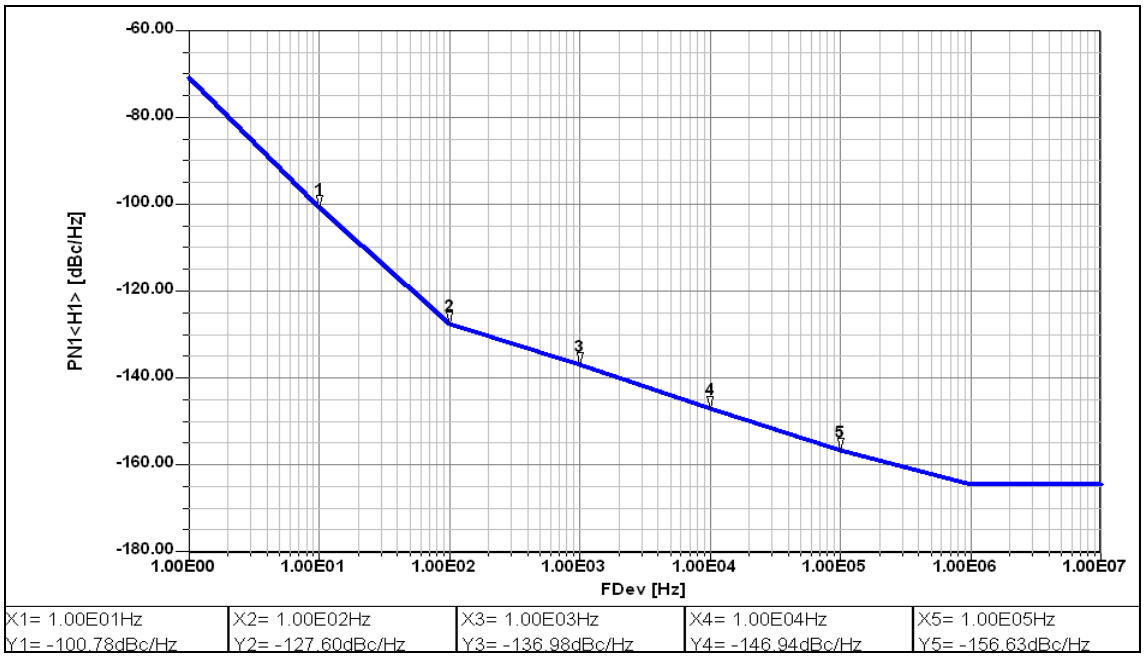


Figure 4: Colpitts oscillator—Phase noise with C1=59pF and C2=59pF

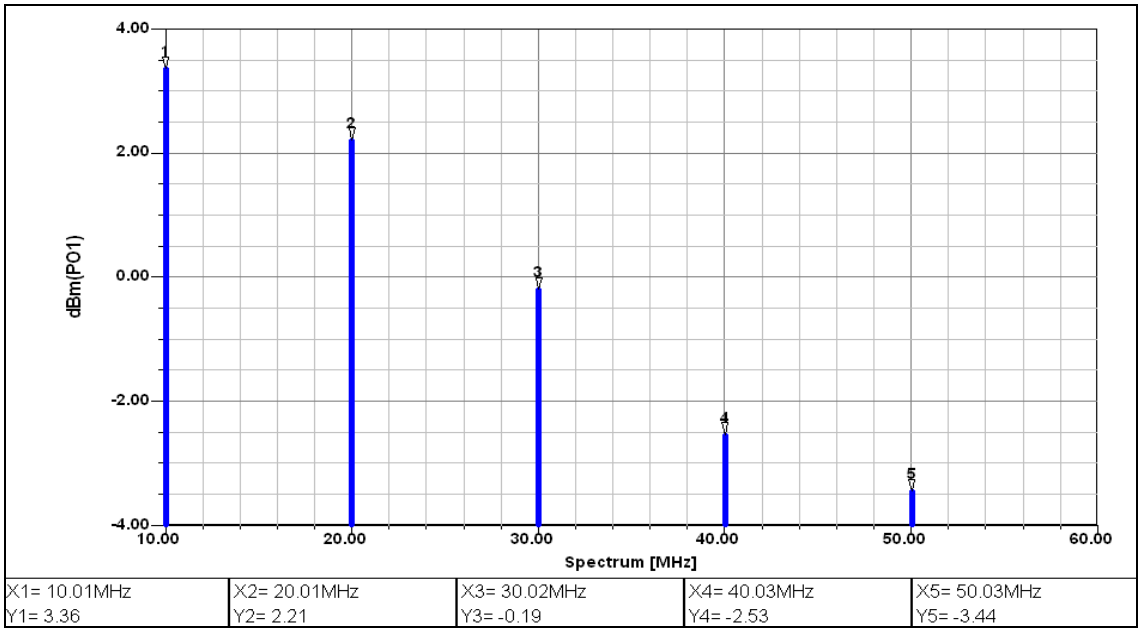


Figure 5: Colpitts oscillator—Output power

Since quartz crystal is mechanical resonator driven by the piezoelectric effect, fundamental and a variety of overtone frequency modes are possible. Unfortunately undesired mode jumping is also possible even in well-planned circuit designs. This problem can be overcome by mode feedback mechanism that not only improves the stability but also improves the phase noise performances by few dB. The feedback resistor R5, which is generally a short at high frequency, gives better performance of phase noise than in a circuit otherwise, assuming there is no flicker noise in the crystal. The complexity on feedback resistor can be

instituted in [3] and [4]. The dynamic mode feedback approach is introduced in reference [3] that includes a methodology for optimum coupling to enhance the dynamic loaded Q, and to reduce or eliminate phase hits, while reducing the thermal drift and susceptibility to micro phonics to an extremely low level, and retaining low phase noise and broadband tunability. A mode feedback coupling is a method in which the crystal is operated in its overtone mode, say the 3rd overtone and then a signal with same amplitude and phase as the 3rd overtone is injected in the resonator such that certain features are canceled and a get better phase noise is obtained.

The adjoining figure show the schematic with the feedback resistor been identified and the change in phase noise due to presence of the resistor as compared to its absence. The presence of the feedback resistor reduces the negative impedance presented by the transistor to the resonator. So the values of the capacitive feedback network can be adjusted in order to set the oscillations.

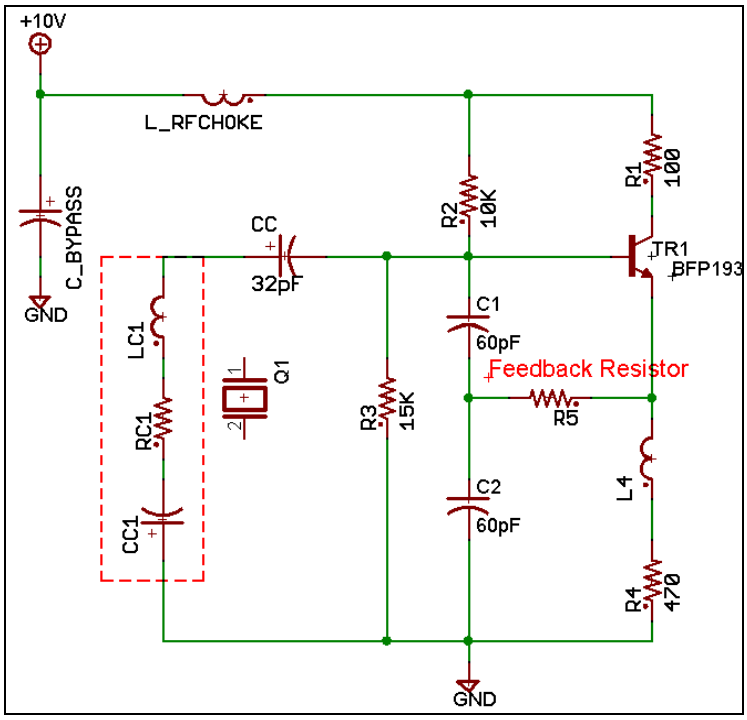


Figure 6: Feedback Resistor

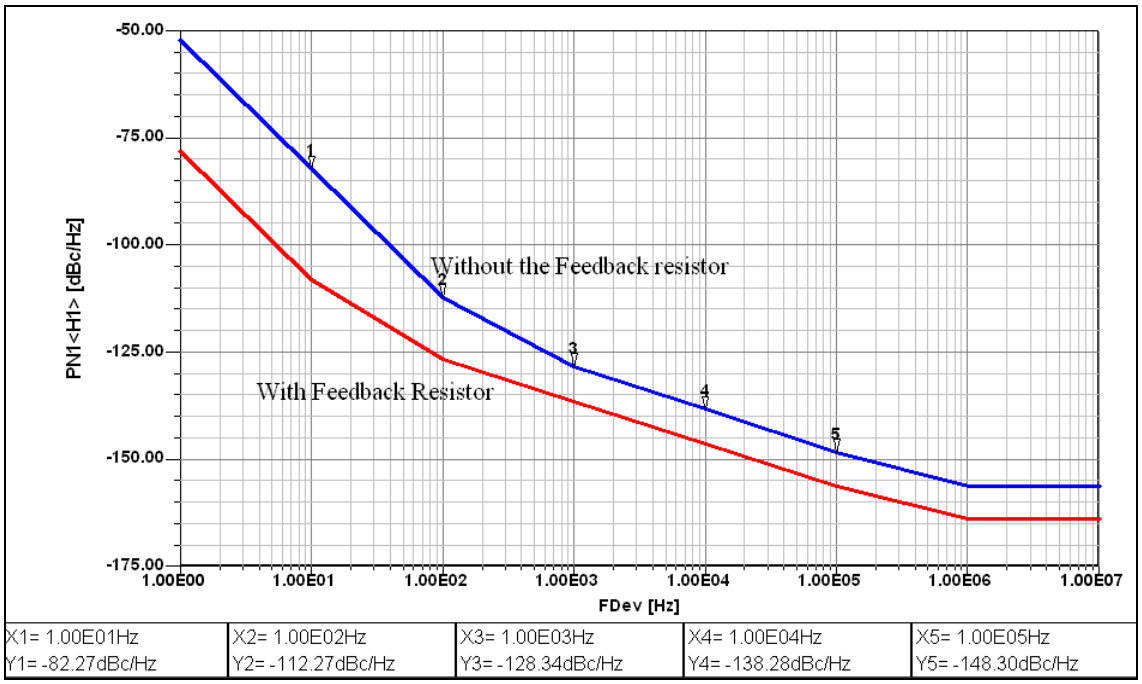


Figure 7: Phase noise of the circuit with and without the feedback resistor.

There are different ways to improve phase noise and the biasing current is one of them. Not only does the proper current will change the phase noise of the oscillator but also the best biasing techniques. We found that given the same current and supply voltage, transistor with fixed biasing gave better results over self-biasing techniques. The voltage feedback form of the stabilized biasing network, or self-biasing technique shown in figure (8), provides voltage feedback to the bias current source resistor RBASE. The base current source is fed from the voltage across the collector-emitter of the transistor V_{ce}, as opposed to the supply voltage V_{cc}. The collector resistor has both I_c and I_b flowing through it The variation in β_{dc}, due to change in the temperature will cause changes in the collector current I_c. Any increase in voltage across R_c will cause V_{ce} to decrease, and this will cause I_b to decrease because the potential difference across the base resistor R_B is decreased. This configuration of the biasing circuit provides negative feedback that tends to reduce the amount by which the collector current increase as β_{dc} is increased due to the rise in temperature, ref [5 pp 219].

$$Ic = \frac{\beta_{DC}\left(V_{CC} - V_{BE}^{'}\right) + I_{CBO}\left(1+\beta_{DC}\right)\left(h_{ie} + R_B + R_C\right)}{h_{ie} + R_B + R_C\left(1+\beta_{DC}\right)}$$

All three temperature-dependent variables, β_{dc}, I_c and V_{ce} influence the collector current due to change in temperature, the derivative of I_c with respect to each factor gives the stability factor for the biasing circuit.

The emitter feedback bias network as in figure (8), where a resistor is connected in series with the device emitter lead to provide the voltage feedback, provides an optimum control over variations in β_{dc} due to variations in temperature and also

from device to device. The emitter resistor must be properly RF bypassed to avoid regenerative effect.

Our example from figure (8) has fixed biasing or the emitter feedback biasing technique. The same circuit was modified to use the voltage feedback biasing of stabilized biasing or the self-biasing technique as shown in figure (8). Both the biasing provided the same collector current of 9.8mA to the oscillator.

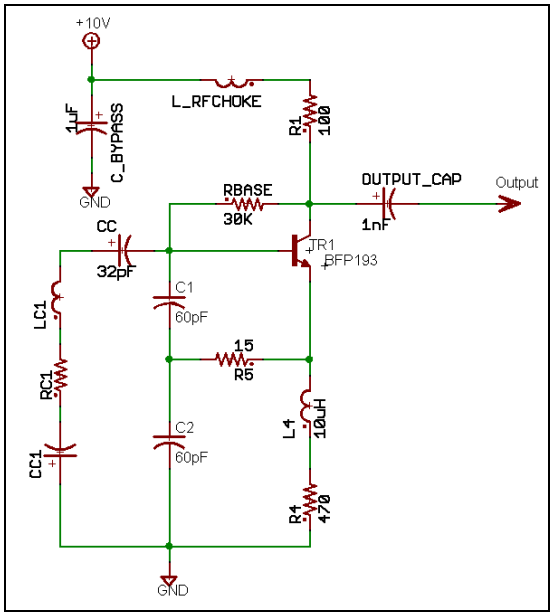


Figure 8: Self biasing for the transistor

The phase noise of the fixed biasing was found to be much better in the close in than that obtained with self-biasing (shown in figure 9).

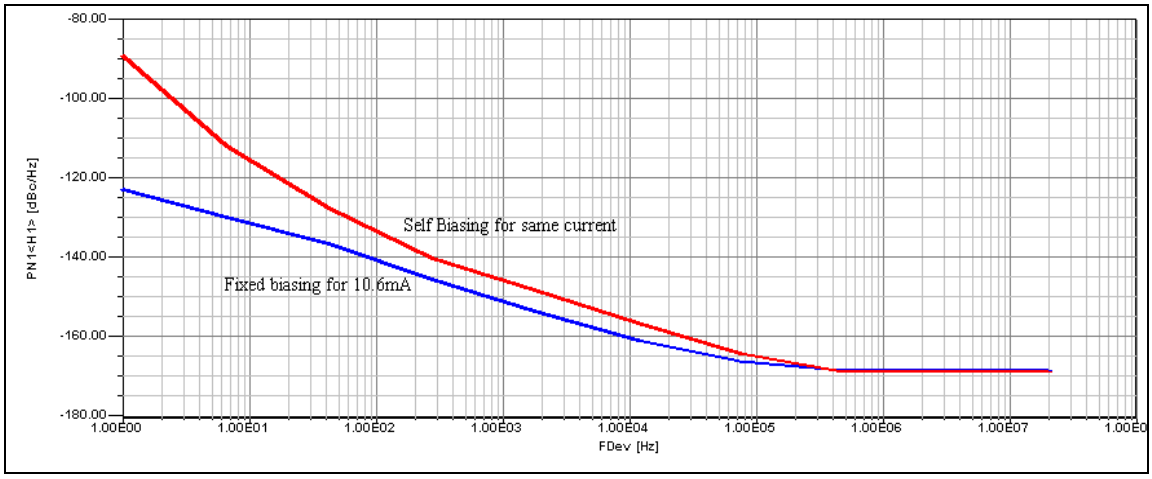


Figure 9: Phase noise comparison between the fixed biasing and the voltage feedback biasing techniques for the transistor.

For further validation silicon N-channel FET based colpitts oscillator was designed with the same current as in the previous example of figure (8). Figure (10) shows the circuit diagram for the FET based oscillator. Traps in the gate-channel depletion layer, traps in the substrates and possibly surface states created by the passivation cause the noise is FET, Ref [7, pp.175]. Much higher 1/f noise occurs in MOSFETs because of the traps in the oxide. Since the noise is voltage noise it is generally plotted as dBv/√Hz. It is found that the BJT has a superior much lower corner frequency, f_c. The GaAs MESFETs will dominate the microwave region but the silicon BJTs will continue to find applications especially for low noise oscillator.

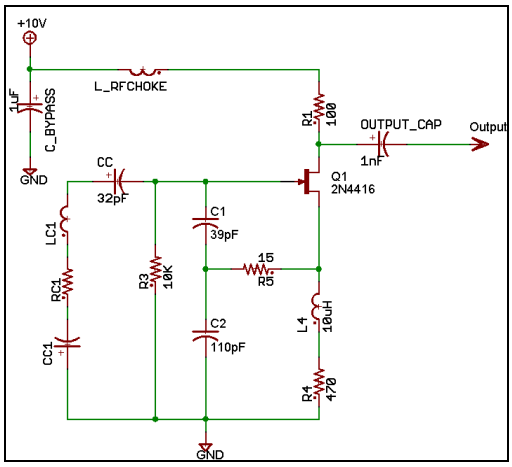


Figure 10: FET oscillator similar to figure (8), same biasing current.

We studied that FET improved the phase noise under same biasing conditions for our example of 10MHz Colpitts oscillator. The output frequency obtained from the BJT was 10.00682MHz and was shifted to a high side when a FET was used. The figure (11) shows the phase noise comparison of using a FET over the BJT for this particular application.

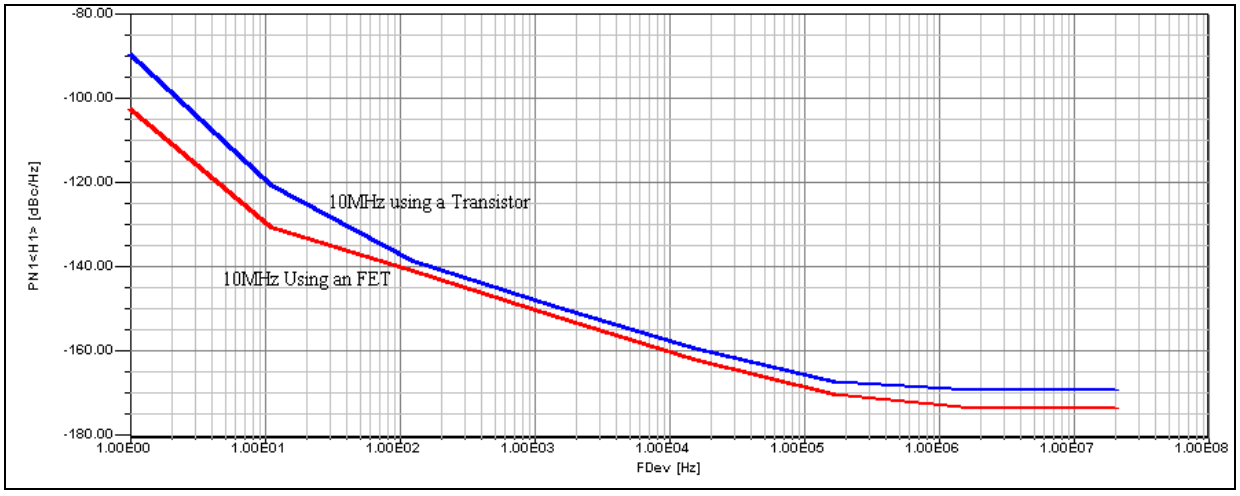


Figure 11: Comparison between using a transistor and FET

A practical circuit was built as per the above design guidelines in Colpitts oscillator configuration. When measured with the circuit values, as shown in figure (12) with the crystal used from Bliley showed a comparable response. The bias was changed and the output stage was connected to amplifier while doing the measurements. The amplifier or the buffer stage of FET does not load the circuit because of the infinite impedance of the FET. The dual gate MOSFET's are the best choice for buffer stage. The simulated results agreed with the measured data. The difference in the phase noise at higher end is due to use of amplifier while measurements. The noise figure of the amplifier raises the noise floor as shown in the simulation plot.

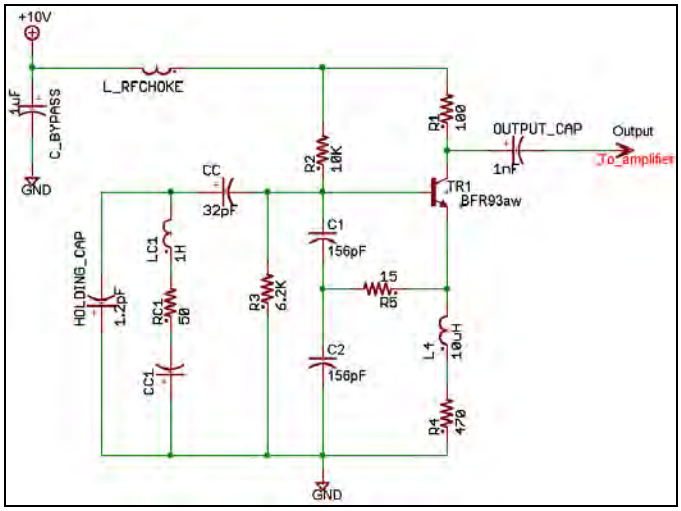


Figure 12: Circuit for of 10MHz oscillator without the Amplifier at the output.

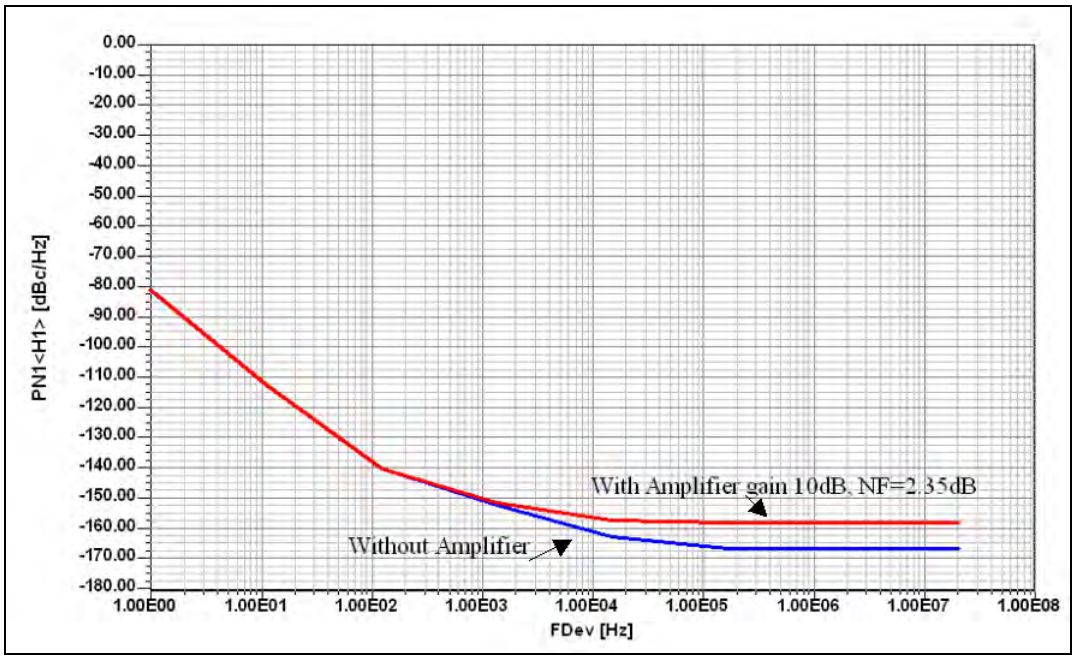


Figure 13: Simulated phase noise of the 10MHz oscillator from figure (12), with and without amplifier at the output, using the Serenade program.

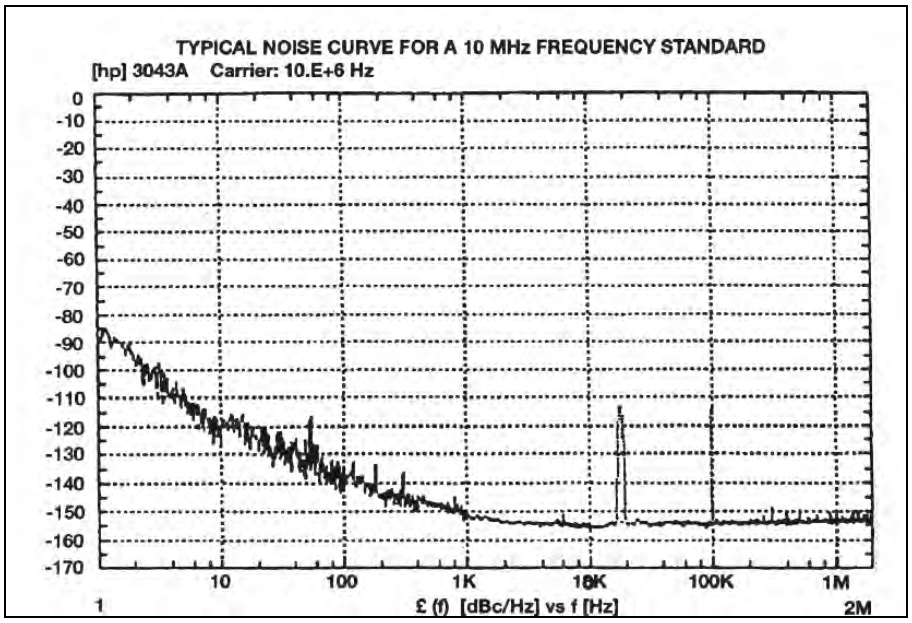


Figure 14: Measured phase noise of the 10MHz oscillator.

Assortments of modifications to the Pierce and Colpitts oscillator are studied in the following section. These modifications are to achieve certain advantages (along with its unwanted disadvantages) over the standard configuration. Shown below is the semi-isolated Colpitts oscillator. Due to coupling of load through Cc, this circuit is not recommended for frequencies above 10MHz at fundamental operational frequency. This limitation of frequency range is due to the miller capacitance at high frequencies. This circuit can be used if instead of the fundamental mode we have an output from the overtones. Characteristics in oscillator also depend from where the output is tapped out. In the normal Colpitts configuration we take the output from the emitter of the transistor. Since there is no collector resistor in the typical Colpitts configuration, the limiting is due to cutoff in transistor. In the normal oscillator the power extracted from the load is much less than the crystal power. More power is extracted only at the expense of loaded Q.

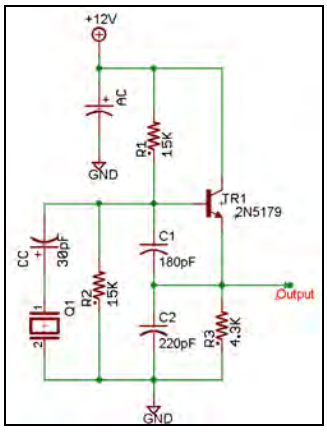


Figure 15: Colpitts oscillator, output from emitter.

In the above examples Figure 12 and Figure 8, and the following two, the output is taken from the collector; such configuration is called the semi-isolated Colpitts configuration. The principal advantage of this configuration is larger output power as compared with the crystal power and better isolation to load than the normal Colpitts configuration. By tuning the collector to harmonic of the oscillator frequency, the circuit acts as frequency multiplier, which gives additional isolation from load to oscillator. Figure (16) is a semi-isolated Colpitts configuration in which a 3.333MHz oscillator gives a tuned output frequency of 10MHz.

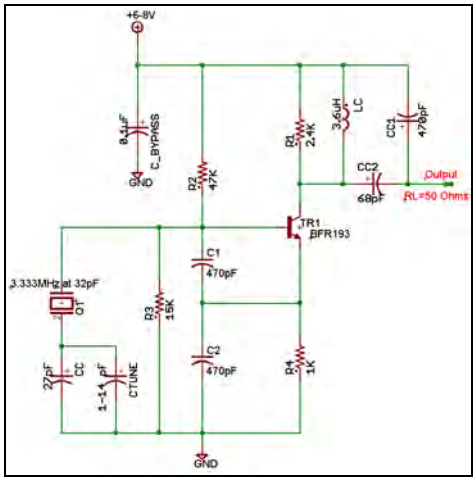


Figure 16: Semi-isolated Colpitts configuration for 10MHz

The output of the semi-isolated Colpitts oscillator can be DC coupled into a common base amplifier in a cascode arrangement. This modification gives excellent isolation to the load and allows much larger collector load in the second transistor. By changing the configuration of the crystal the output current can be forced to flow through the resonator, which reduces the noise floor considerably.

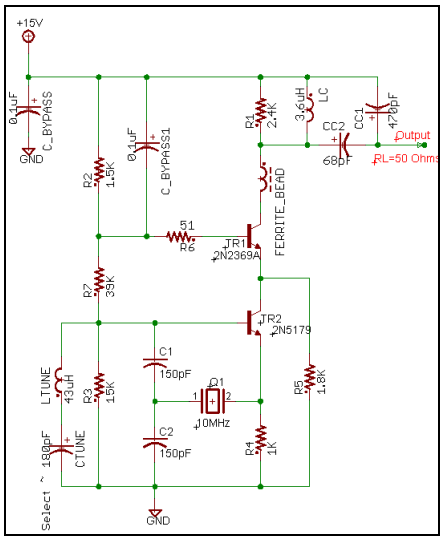


Figure 17:Modified Semi-isolated Colpitts, 10MHz oscillator in Cascode configuration.

Another example of the Colpitts oscillator is the configuration in which the power is extracted from the resonator, reference [20]. By extracting the resonator power from crystal the crystal acts as a very narrow band filter on noise generated by the oscillator stage. A schematic with FET operating for 5MHz operational frequency is shown in figure 18.

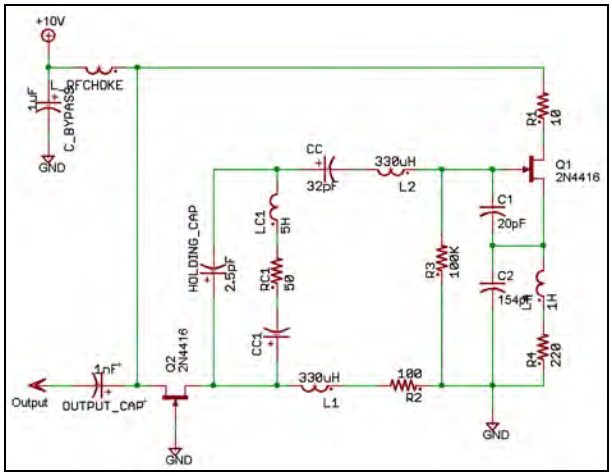


Figure 18: A Modified Semi-isolated Colpitts oscillator for 5MHz in which the power is extracted from resonator.

Since a common base stage has very low input impedance at the emitter, the Q degradation will be very slight. The principal disadvantage of this circuit is that the output power will be a small percentage of the crystal power. This may cause poor floor noise or high crystal power dissipation, but this configuration gives better harmonic rejection and good isolation.

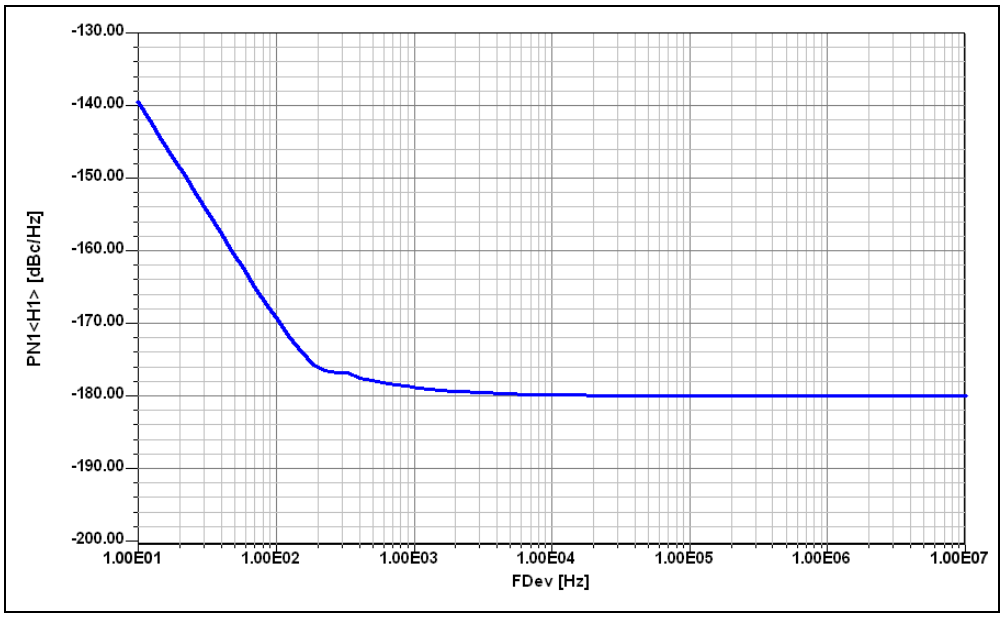


Figure 19: A Modified Colpitts oscillator with power extracted through resonator for 5MHz.

The noise parameter for FET was not considered.

Low-frequency crystals have thicker and large quartz wafers and ranges in few Henrys, whereas, high-frequency crystals have thinner and smaller quartz wafers and ranges in a few micro Henrys. Starting at about 30 MHz, the quartz becomes so thin that it is hard to handle during the manufacturing process. Inverted "mesa crystals" allow crystal to resonate at higher fundamental mode frequency (above 30 MHz) but manufacturing process is not cost-effective with respect to oscillator stability and phase noise performances.

The promising alternative is overtone mode, which is similar in concept to a harmonic, with the exception that crystal oscillation overtones are not exact integer multiples of the fundamental. An overtone-mode crystal cannot be used in a fundamental-mode oscillator, and vice versa, it may oscillate but not at the correct frequency and exhibit poor stability.

As an example, Figure 20(a), a 100 MHz crystal resonator based Colpitts oscillator was designed according to a set of specifications that included +13 dBm output power, 50-Ω load, and phase noise of –132 dBc/Hz offset 100 Hz from the carrier, with the intention of applying the new approach to this basic design to determine the component parameters that mostly affect the phase noise performance for a given class and topology. For this typical design example, an NE68830 transistor from NEC was selected for validation. Revising the design procedure for this particular design we have the following steps.

The first step in the design process involved calculating the operating point for a fixed normalized drive of x = 20, as described earlier. The output voltage and

current at the fundamental frequency (f_0, $\omega_0 = 2\ f_0$), based on the output-power requirement, can be given by

$$V_{out}(\omega_0) = \sqrt{P_{out}(\omega_0) * 2R_L} = \sqrt{20E - 3 * 2 * 50} = 1.414V$$

$$I_{out}(\omega_0) = \frac{V_{out}(\omega_0)}{50} = 28.3mA$$

$$\left[I_E(\omega_0)\right]_{x=20} = \left[I_{E1}(\omega_0)\right]_{x=20} + \left[I_{E2}(\omega_0)\right]_{x=20} = 2I_{DC}\left[\frac{I_1(x)}{I_0(x)}\right]_{x=20} \approx 56mA$$

$$\left[I_{E1}(\omega_0)\right]_{x=20} = I_{out}(\omega_0) = 28.3mA \text{ (O/P current to the load)}$$

$$\left[I_{E2}(\omega_0)\right]_{x=20} = \left[I_E(\omega_0)\right]_{x=20} - \left[I_{E1}(\omega_0)\right]_{x=20} = 27.3mA$$

$$I_{E-DC} = \frac{\left[I_E(\omega_0)\right]_{x=20}}{2\left[\frac{I_1(x)}{I_0(x)}\right]_{x=20}} = 28.3mA$$

The second step in the design process involved the development of the biasing circuit. For the best close-in phase noise, a noise-feedback DC circuit is incorporated to provide the desired operating DC conditions with I_E = 28.3 mA, V_{CE} = 5.5 V, supply voltage, V_{cc} = 8 V, $\beta \approx 120$, and $I_B \approx 0.23$ mA.

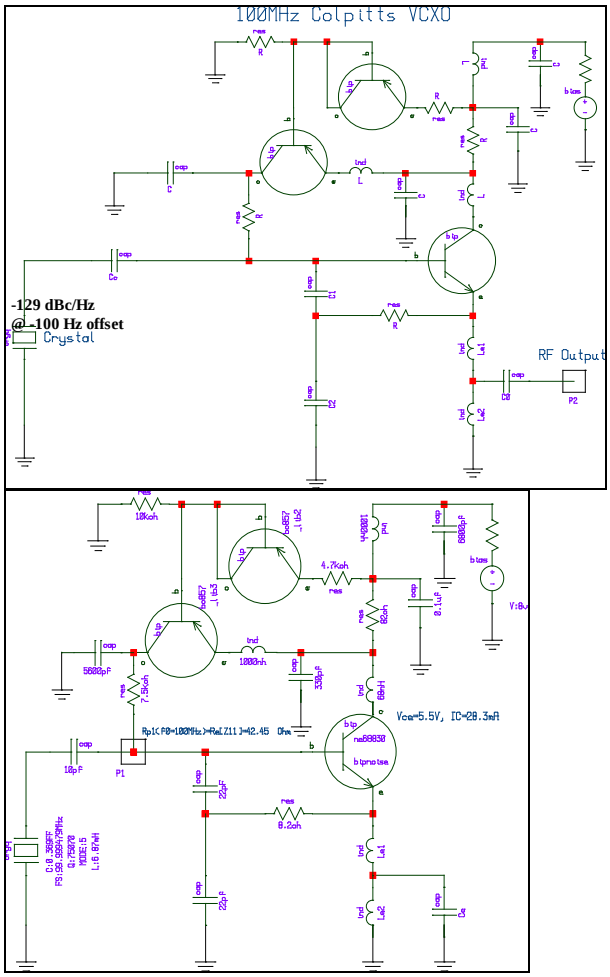


Figure 20: (a) 100MHz VCXO (tuning diodes and holder capacitance canceling inductance are missing for simplification), (b) Loss resistance R_{p1} (Port: P_1).

The third step involves calculating the large-signal transconductance Y_{21}

$$Y_{21}\big|_{\lg} = G_m(x) = \frac{qI_{DC}}{kTx}\left[\frac{2I_1(x)}{I_0(x)}\right]_{f=fundamental}$$

$$\left[Y_{21}\right]_{\omega=\omega_0} = \left[\frac{1.949I_{E-DC}}{520mV}\right] = 107mS$$

The fourth step in the procedure involves the calculation of loop gain and equivalent loss resistance as

$$Loop-Gain = [LG]_{sustained-condition} = \left[\frac{R_{p1}(f_0)Y_{21}(x)}{n}\right] = \left[\frac{Rg_m}{x}\right]\left[\frac{2I_1(x)}{I_0(x)}\right]\left[\frac{1}{n}\right] > 1$$

$$R_{p1}(f_0) = \mathrm{Re}[Z_{11}] = 42.45\Omega$$

where, $R_{p1}(f_0)$ is the equivalent resistive load across the port 1 (Figure 20b). For practical purpose, the loop gain should be 2.1 to achieve good starting conditions for stable and guaranteed oscillation.

$$n = \left[\frac{R_{P1}(f_0)Y_{21}(x)}{Loop-Gain}\right] = \frac{0.107\times 42.45}{2.1} \approx 2.16$$

The fifth step in the design procedure involves calculation of the feedback capacitor ratio based on transformation factor, n as

$$n = 1+\left[\frac{C_1}{C_2}\right] = 2.16 \Rightarrow \left[\frac{C_1}{C_2}\right]_{x=20} = 1.16$$

The sixth step involves calculation of the absolute value of the feedback capacitor based on the input impedance Z_{in} (looking into the base of the transistor). The expression for Z_{in} is given as

$$Z_{in} \cong -\left[\left(\frac{Y_{21}}{\omega^2(C_1^*+C_p)C_2}\right)\left(\frac{1}{(1+\omega^2Y_{21}^2L_p^2)}\right)\right] - j\left[\left(\frac{(C_1^*+C_P+C_2)}{\omega(C_1^*+C_P)C_2}\right) - \left(\frac{\omega Y_{21}L_P}{(1+\omega^2 ii Y_{21}^2L_p^2)}\right)\left(\frac{Y_{21}}{\omega(C_1^*+C_P)C_2}\right)\right]$$

where, C_P = (C_{BEPKG} +Contribution from layout)=1.1pF, L_P=(L_B + L_{BX} +Contribution from layout)=2.2nH. The expression for the negative resistance (R_n, without parasitic) can be described by

$$R_{neq} = \frac{R_n}{(1+\omega^2Y_{21}^2L_P^2)} \cong \frac{R_n}{1.0218}$$

$$R_n = -\left[\frac{Y_{21}^{+}}{\omega^2C_1C_2}\right]_{x=20} = \frac{0.107}{(2\pi\times 1\times 10^8)^2C_1C_2}$$

For sustained oscillation $\rightarrow$ Rneq $\geq$ 2RP1(f0) $\cong$ 84.9Ω

$$R_n \geq 1.0218\times 84.9 \cong 86.76\Omega$$

$$\therefore \quad C_1C_2 \leq \left[\frac{1}{(2\pi\times 1\times 10^8)^2}\right]\left[\frac{0.107}{86.76}\right] \approx 3.13\times 10^{-21}$$

$$C_1 = 25pF = [C_1^* + C_P] \Rightarrow C_1^* = C_1 - C_P = 23.84pF, \quad C_2 = 22pF$$

For practical purpose, C_1^*=22pF. The sixth step is to determine noise factor (F), which is needed prior for the evaluation of the phase noise and the final step in the approach involves calculating the phase noise.

The calculated phase noise at 100 Hz offset from the carrier frequency of 100MHz is –132 dBc/Hz (Q=100,000).

Figure-20 incorporates the component values as per above design calculations and figures 21 and 22 shows the simulated phase noise and output power for 100 MHz crystal oscillators. Simulated and calculated data of the oscillator agrees within 2-3dB.

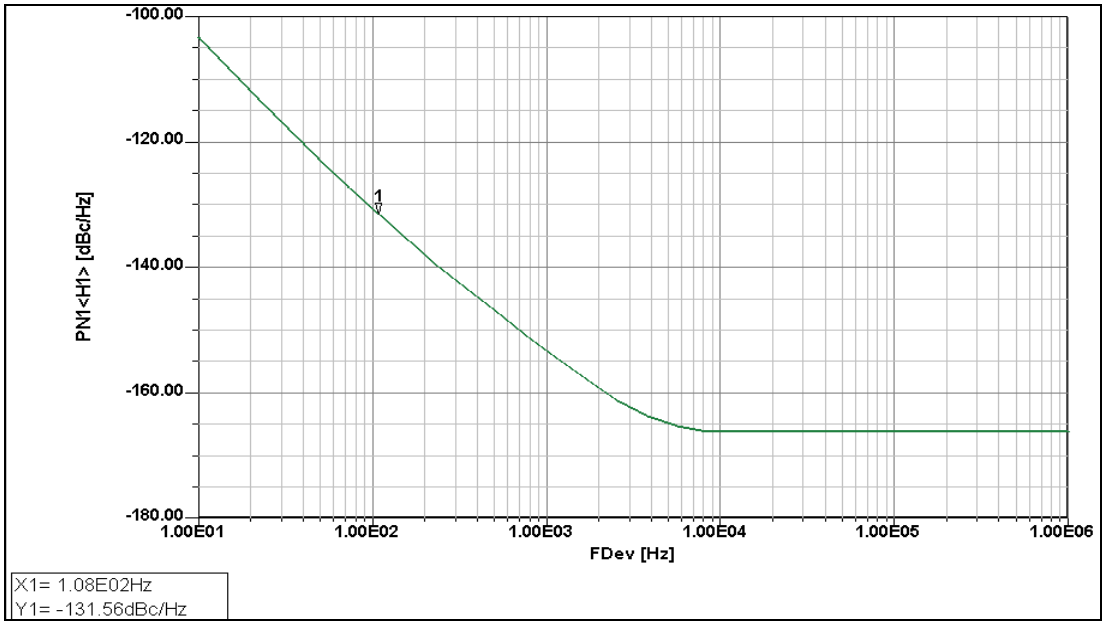


Figure 21: Simulated phase noise plot of 100MHz VCXO

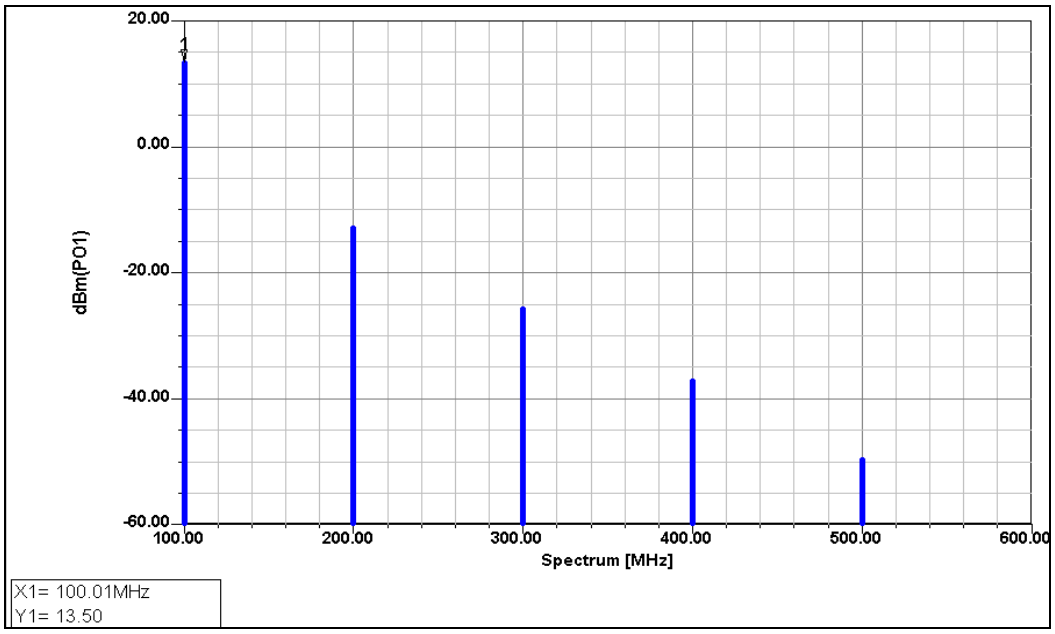


Figure 22: Simulated O/P power plot of 100MHz VCXO

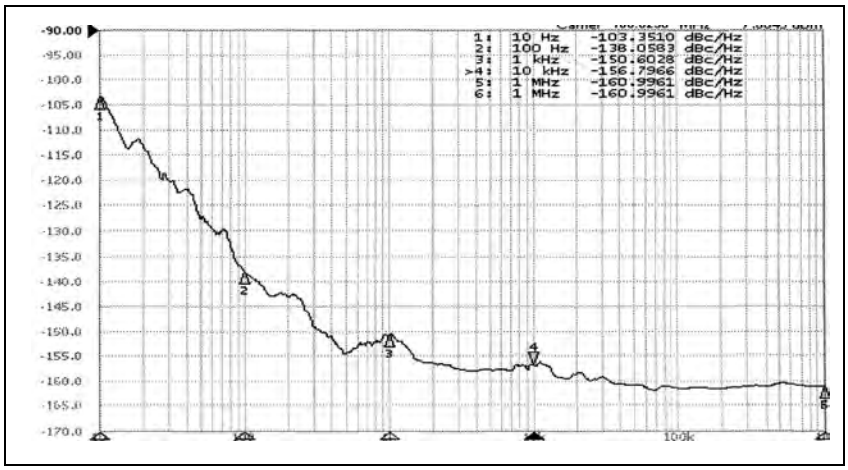


Figure 23: Measured phase noise plot of 100MHz VCXO

A Butler oscillator, or the bridged-T oscillator, is the most popular member of a family of oscillators where the emitter current is the current through the resonator, or crystal. As the current flows through the crystal it is much sinusoidal and the harmonic contents are reduced to a large extent. This filtering action improves the phase noise outside the effective bandwidth of the crystals, resonant frequency, f, by operating Q.

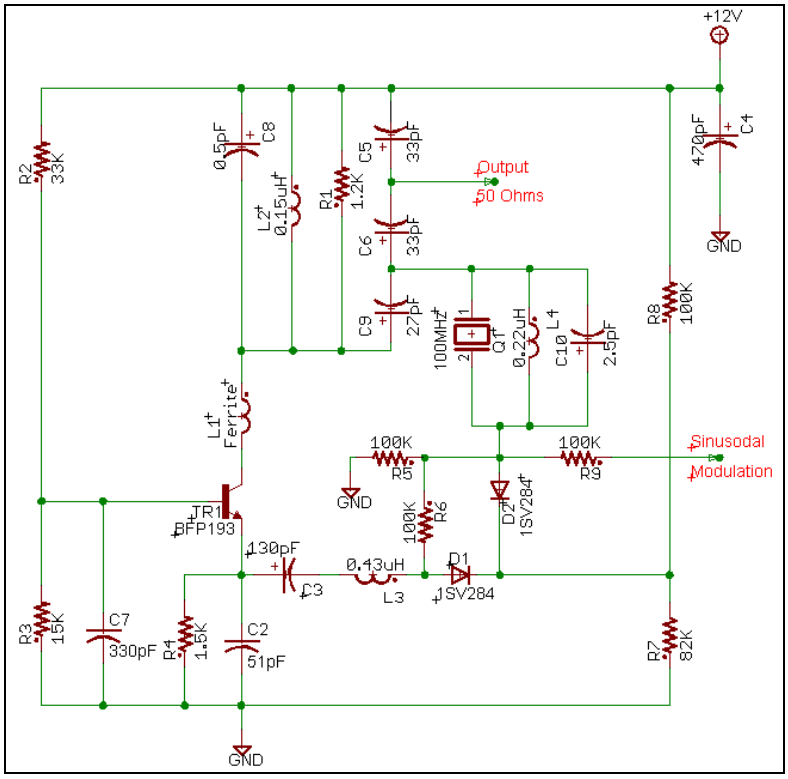


Figure 24: 100MHz 5th Overtone oscillator in Butler Configuration

The circuit in figure 24 shows a design of a 5th overtone 100 MHz crystal oscillator. In this case, the collector impedance for the other responses is very low, and the oscillations can be sustained only at the fifth mode.

The crystal holding capacitor *C0* is tuned out by L4 (0.22uH inductor in figure 24) is used to tuned out any spurious oscillations that can occur. This also greatly improves the voltage linearity of the output response. The circuit is forced to the desired output frequency by the collector tank for any susceptible oscillations, if any.

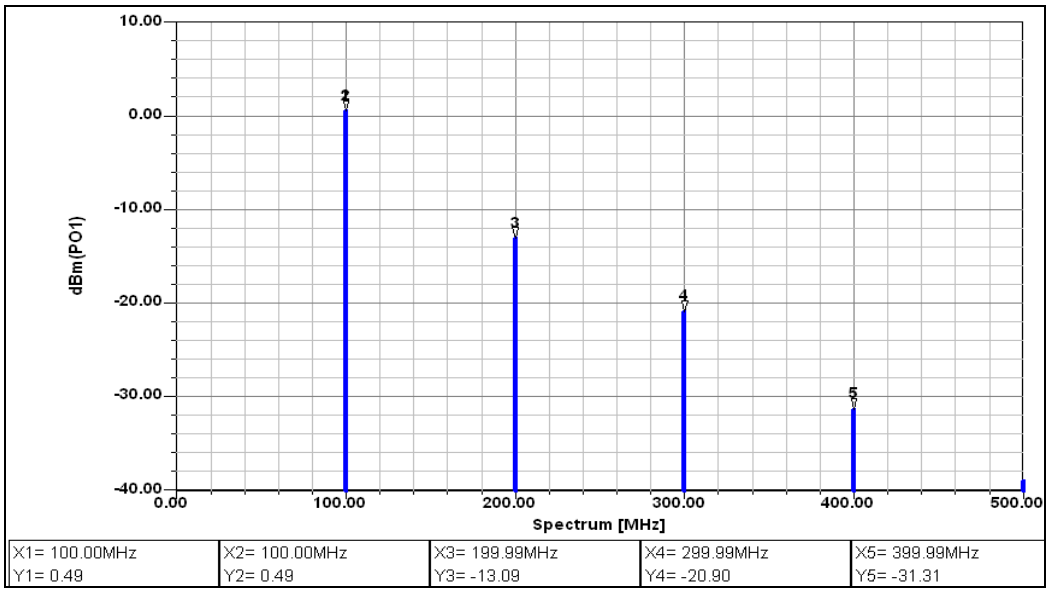


Figure 25: Output of 100MHz 5th overtone Butler oscillator

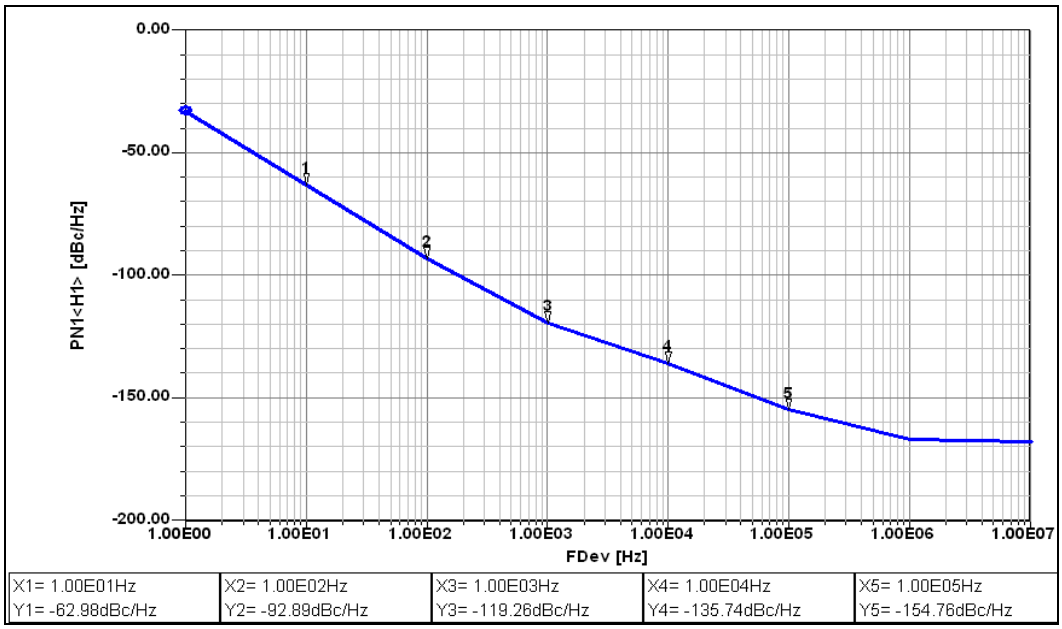


Figure 26: Phase noise of the 100MHz Butler oscillator.

The Pierce oscillator can also be modified as the Colpitts oscillator and the output power is extracted from the resonator while the crystal operates at series resonance. The collector of the transistor is not tuned to fundamental frequency of operation. Since the effective collector load must be capacitive, parallel resonance must be set lower than the frequency of operation. If the collector tank is tuned to a frequency between the fundamental and the overtone, the circuit will look inductive at the fundamental frequency and capacitive at the third overtone. Hence the circuit can operate only on the overtone. In this configuration the crystal filters the output signal and the oscillator transistor is operating in potentially lower noise configuration. The crystal current is lower than the circulating current in the loop, so the output is low. The low power into base stage may cause poor floor or high crystal power dissipation.

The capacitor C3 and inductor L3 forms the trap for fundamental frequency so that the oscillator can operate in the 3rd overtone mode. The nominal values are designed and capacitor C3 is made to be test on select so that proper oscillations are set. For our example C3 equal to 96pF was required to get the proper oscillations. The phase noise and the output power as a function of frequency is plotted in accompanying figures.

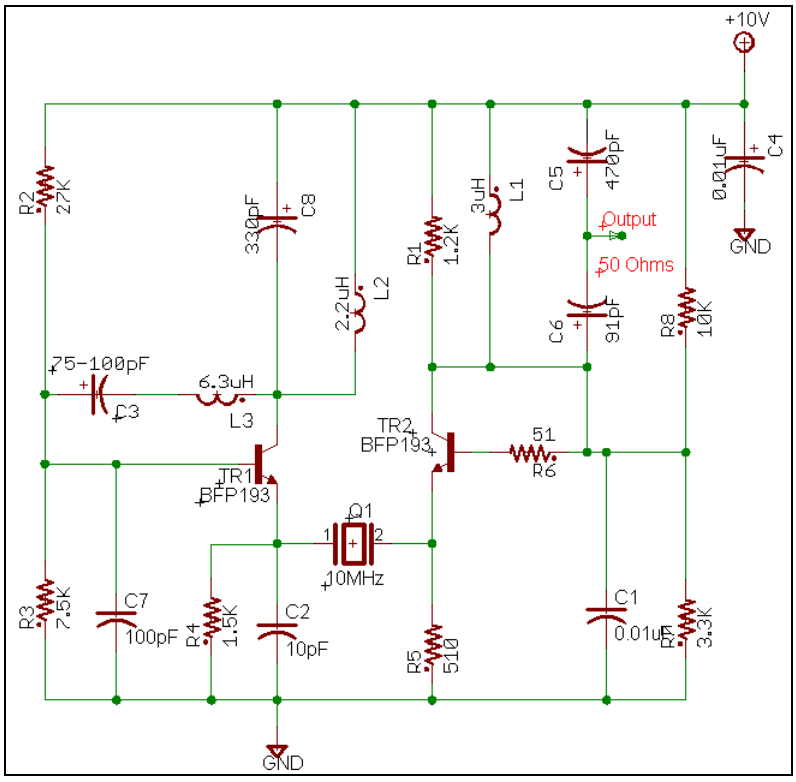


Figure 27: 10MHz 3rd overtone oscillator in Pierce Configuration

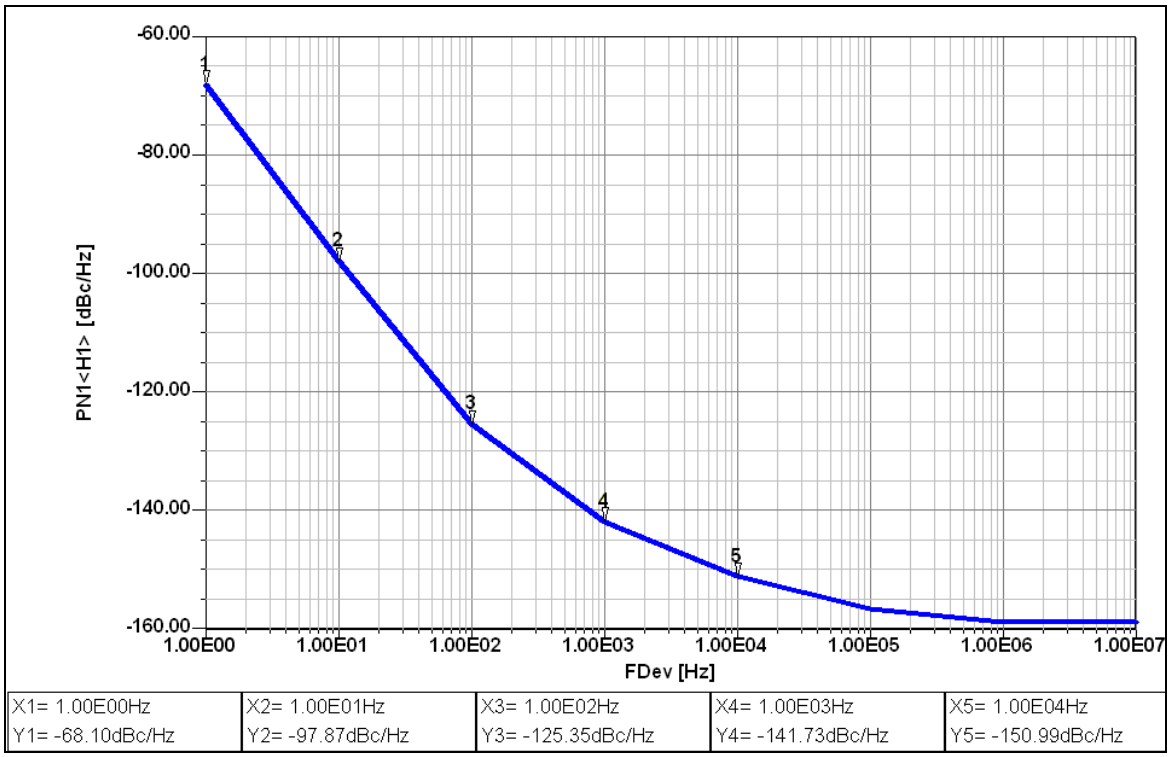


Figure 28: Phase noise response for 10MHz Pierce configuration oscillator.

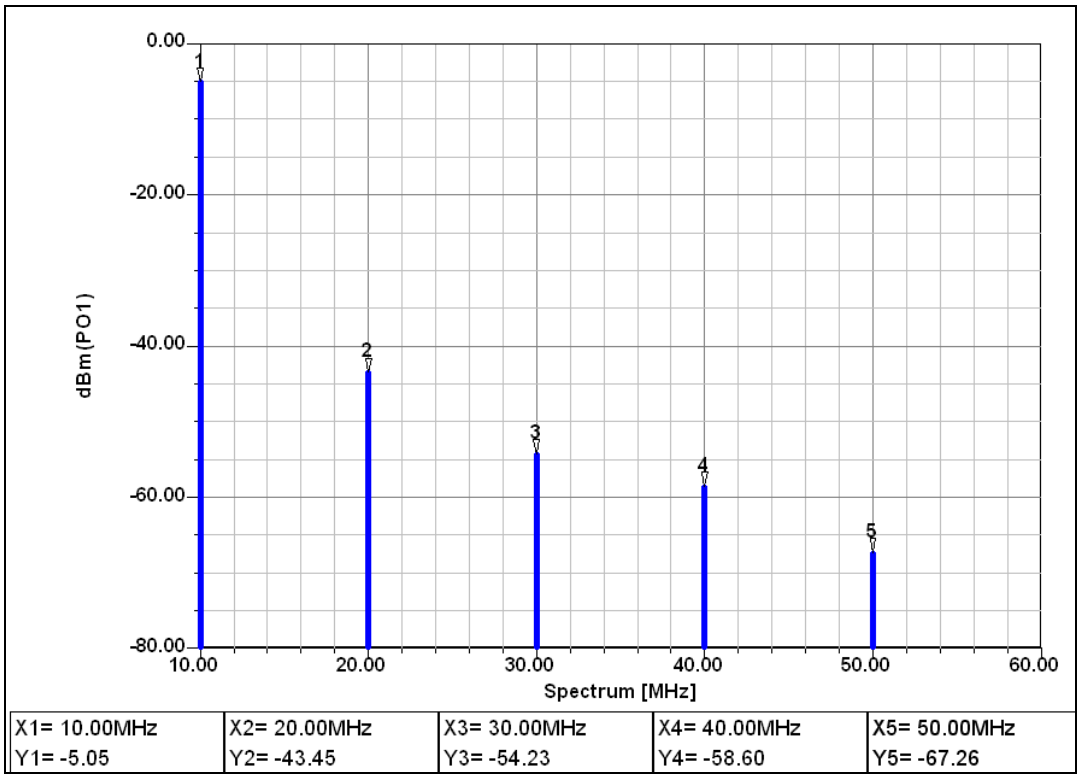


Figure 29: Output response for 10MHz Pierce configuration oscillator.

Limiting action: As we all know that the oscillator is an autonomous circuit. The noise signal in the active device or the transient from the power supply turn-on gets amplified, and continues to grow till it reaches the limiting action of the nonlinearities present in the circuit that provides the stable oscillations. This limiting action could be a result of the biasing done on the active device that controls the oscillating frequency or can be imposed from certain external means like Automatic Level Control (ALC).

The limiting action can be seen as the fundamental component of collector current, which is expressed as Fourier series, gets reduced by base-emitter voltage swing or by the collector-emitter voltage swing. The collector current, I_c, is expressed as a function of temperature and V_{be}, base-emitter voltage.

$$i_e(t) = I_s e^{\frac{qv_{be}(t)}{kT}}$$

$$v_{be}(t) = V_{BE} + v1\cos(\omega t)$$

$$i_e(t) = I_s e^{\frac{q(V_{BE}+v1\cos(\omega t))}{kT}} = I_s e^{\frac{qV_{BE}}{kT}} e^{\frac{qv1\cos(\omega t)}{kT}} = I_s e^{\frac{qV_{BE}}{kT}} e^{x\cos(\omega t)}$$

$$e^{x\cos(\omega t)} = \sum_n a_n(x)\cos(n\omega t) = I_0(x) + \sum_{n=1}^{\infty} I_n(x)\cos(n\omega t)$$

$$i_e(t) = I_s e^{\frac{qV_{BE}}{kT}}\left(I_0(x) + \sum_{n=1}^{\infty} I_n(x)\cos(n\omega t)\right) = I_s I_0(x) e^{\frac{qV_{BE}}{kT}}\left(1 + \sum_{n=1}^{\infty}\frac{I_n(x)}{I_0(x)}\cos(n\omega t)\right)$$

$$= I_{DC}\left(1 + 2\sum_{n=1}^{\infty}\frac{I_n(x)}{I_0(x)}\cos(n\omega t)\right)$$

where, I_{DC} is the dc emitter current, $I_n(x)$ is the modified Bessel function, I_s is the device saturation current, $v_{be}(t)$ is the drive voltage across base-emitter junction, V_{BE} is the dc base-emitter voltage and $v1\cos(\omega t)$ is the drive signal voltage. This exponential nature causes emitter current $i_e(t)$ to be composed of pulses the width of which decreases sharply as magnitude of $v_{be}(t)$ increases. For further understanding it is recommended to read the chapter 6 of reference 5.

The limiting action occurs due to the cut-off of the emitter current during part of the cycle because of the swinging of the base emitter junction below the contact potential. A colpitts oscillator design based on base-emitter voltage limiting is discussed below. The design values were computed using the algorithm presented by Benjamin Parzen. The load resistor obtained by this algorithm was 2.23KΩ and so a transformer was used to match with standard 50Ω load.

The schematic and the output phase noise simulated are shown in the adjoining figures. The design is more or less similar to the steps listed above except for the way the capacitance is computed here.

$$C1 = \frac{159000}{X1 * f}(pF)$$

$$X1 = \frac{v1}{I_1(x)}$$

$$Cb = C1 - \left(C_{bed} + C_{1M} + C_{bet}\right)(pF)$$

$$C_{1M} = C_{cb}\left(1 + \frac{V_L}{v1}\right)$$

$$C_{bed} = \frac{gm * 159000}{f_T}$$

$$Cn' = C_N - C_{cb}\left(1 + \frac{v1}{V_L}\right) - C_{ce}\ (pF)$$

$$C_N = \frac{159000}{XC_N * f}(pF)$$

$$XC_N = (1 - 0.2^2)\sqrt{\left(\eta R_{df} - \frac{R_{df}^2}{R_L}\right)R_L}$$

where, $X1$ is the drive dependent impedance, f is the operating frequency, C_{bet} is the total base-emitter capacitance, C_{cb} is the collector-base capacitance, V_L is the voltage across the load, R_{df} is the change in the resistance of resonator with slight variation in frequency, η is the power efficiency, gm is the large signal transconductance, f_T transition frequency of the transistor and R_L is the load resistor.

Based on the following equations a colpitts oscillator circuit was designed that uses the base-emitter limiting and the phase noise and output power was simulated.

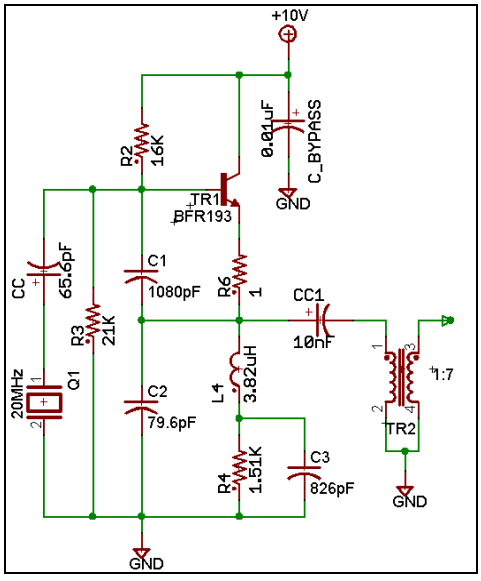


Figure 30: Colpitts schematic of 20MHz crystal oscillator implementing emitter-base limiting action.

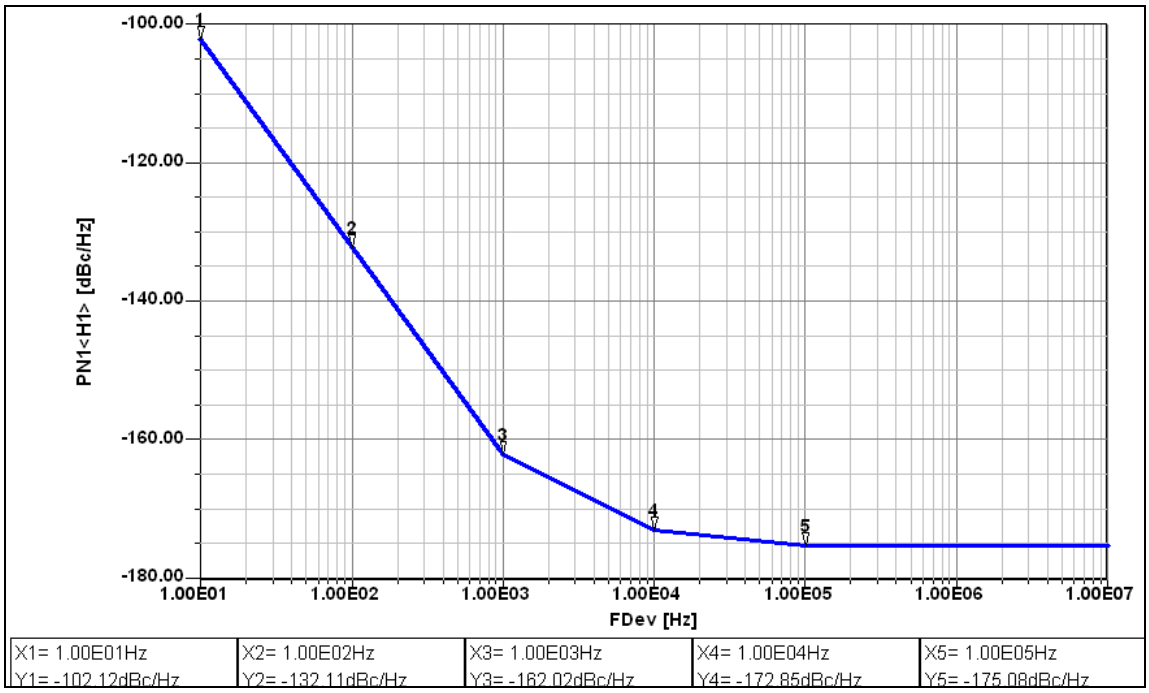


Figure 31: Phase noise response for 20MHz Colpitts-crystal oscillator implementing emitter-base limiting action.

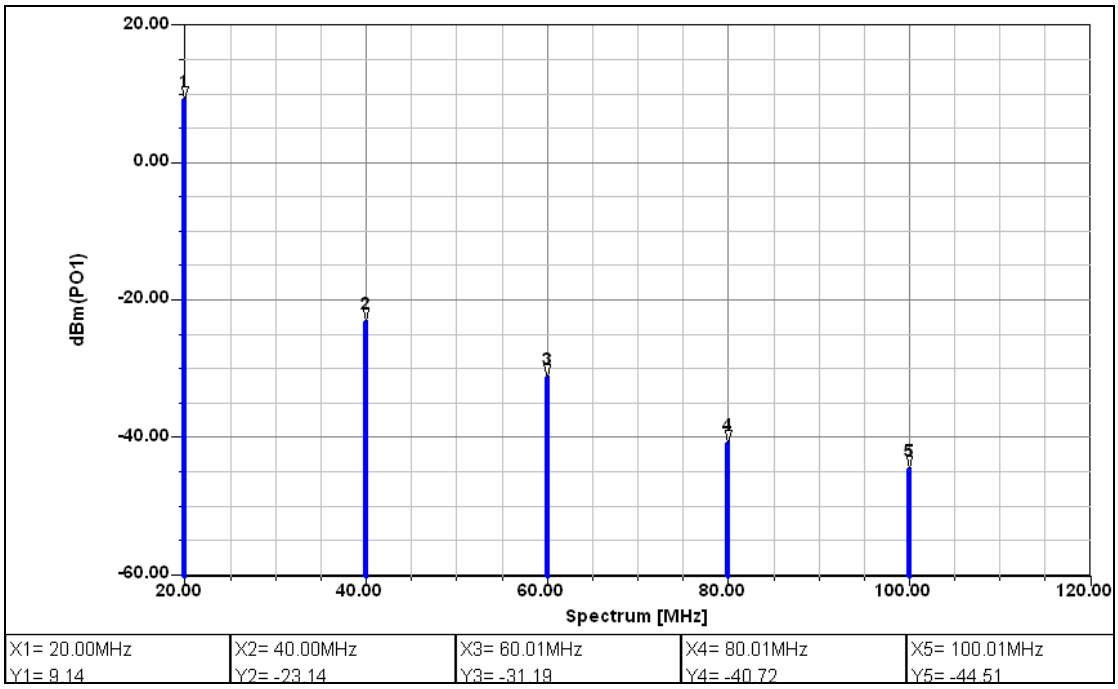


Figure 32: Simulated output response for 20MHz Colpitts-crystal oscillator implementing emitter-base limiting action.

Colpitts oscillator using the collector-base voltage limiting is discussed in short below. A major difference between the emitter-base limiting action over the collector-base limiting action is the overall power consumption. The supply current required is increased in collector-base limiting action due to greater loss in the resonator. Also the operational Q is lower in collector-base limiting action.

A circuit with collector-base voltage limiting action is implemented and shown in the figure 32. The design equations and algorithm can be referred from Ref. [8, chapter 6, 9].
The simulated phase noise and the output response are shown from the Ansoft serenade program.

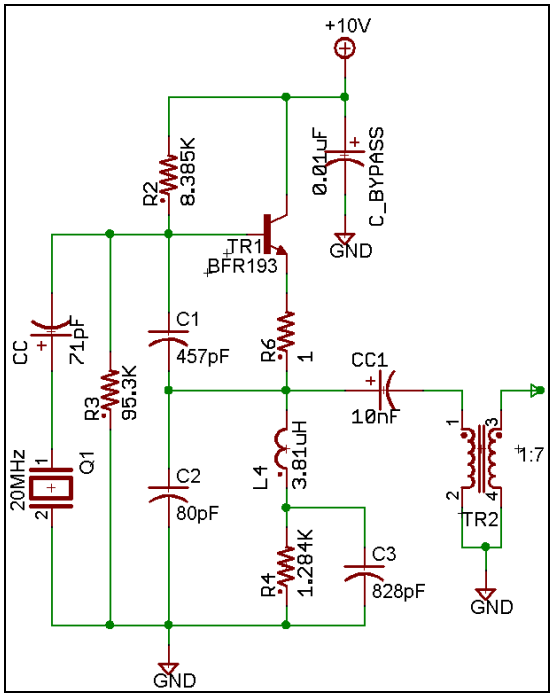


Figure 33: Colpitts schematic of 20MHz crystal oscillator implementing collector-base limiting action.

Few points of differentiation in the two limiting actions can be summarized as below. The base-emitter cutoff limiting is superior to collector-base limiting as long as the resistive impedance of the manufactured crystal is constant. As soon as the resistance change it will be difficult to have a production run of these designs. The change in the resonator impedance will have to be manually compensated. The emitter-base limiting has better supply sensitivity over collector-base designs. This is an advantage with the collector-base limiting action due less labor required. When the supply current is changed in base-emitter we can predict the direction of change and frequency changes can be compensated, while is collector-base limiting action the change of frequency will be difficult to predict. The base-emitter limiting action will give less degradation to the operating Q of the circuit, and provide higher frequency operation due to larger collector-emitter voltage. For lower drive level voltage to operate the

crystal, the base-emitter limiting action should be used as it becomes more difficult to maintain all the biasing voltage constant.

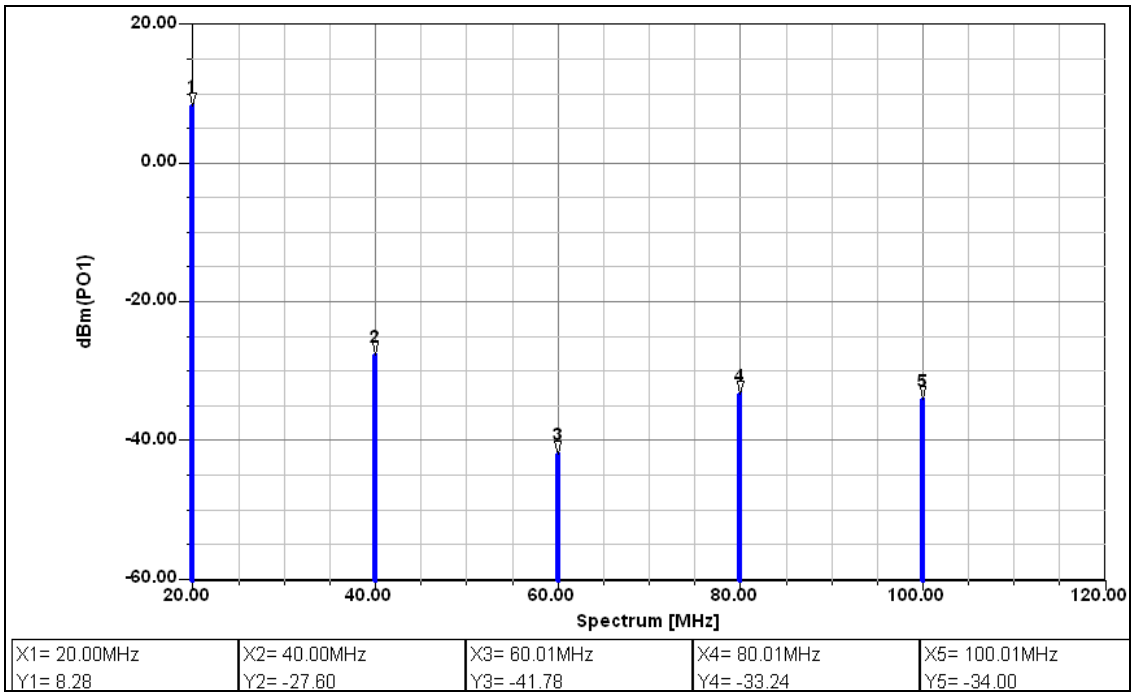


Figure 34: Phase noise response for 20MHz Colpitts-crystal oscillator implementing collector-base limiting action.

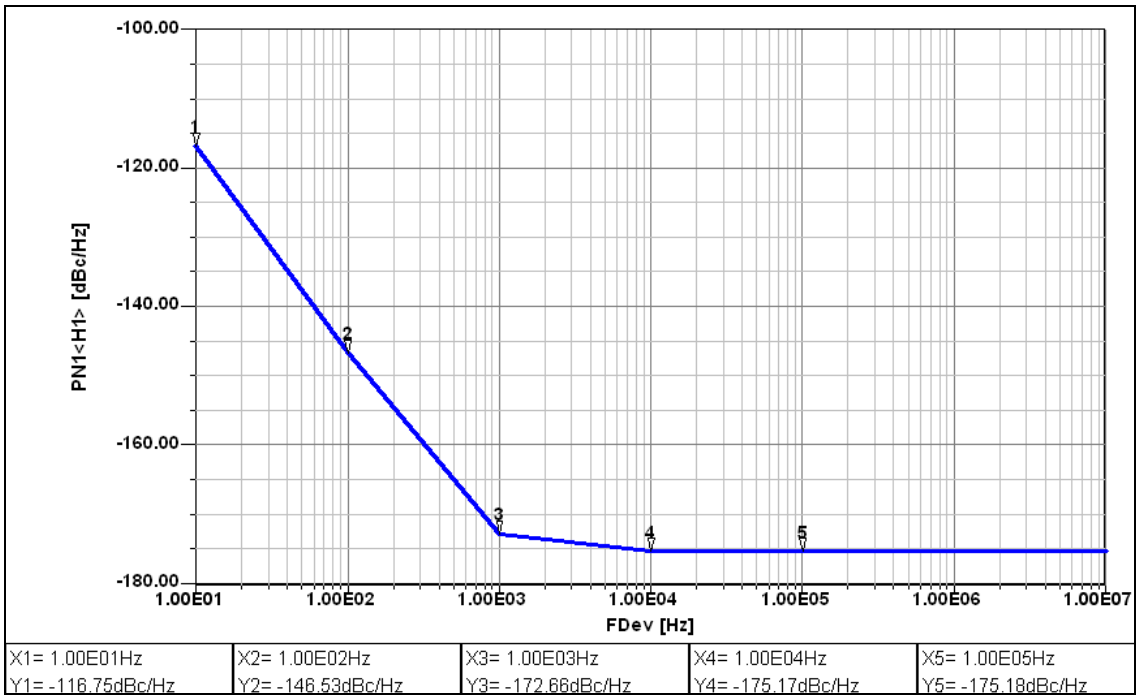


Figure 35: Simulated output response for 20MHz Colpitts-crystal oscillator implementing collector-base limiting action.

Another example of butler oscillator is the following circuit from [8]. The algorithm from Parzen was used to compute the required values of components (not standard components).

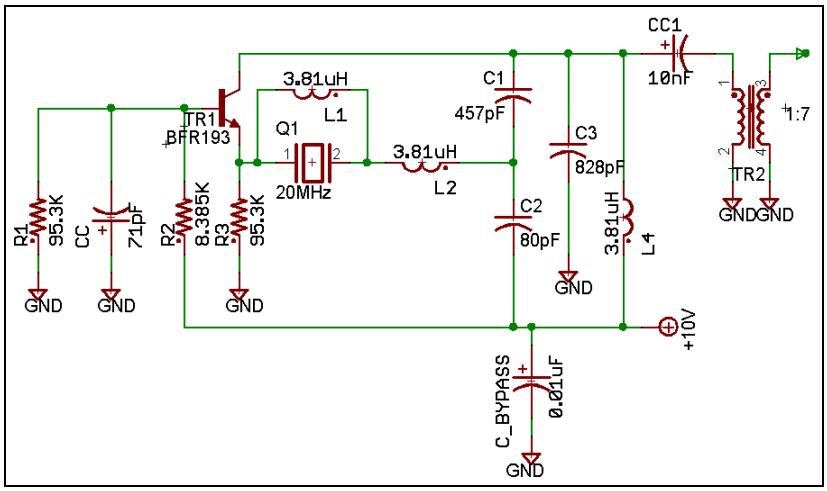


Figure 36: 20MHz Butler-crystal oscillator.

The circuit of 20MHz butler oscillator was simulated in CAD software and the simulated response of phase noise and output power are as shown in the adjoining figure. The transformer was used at the output to match the impedance to 50 ohm.

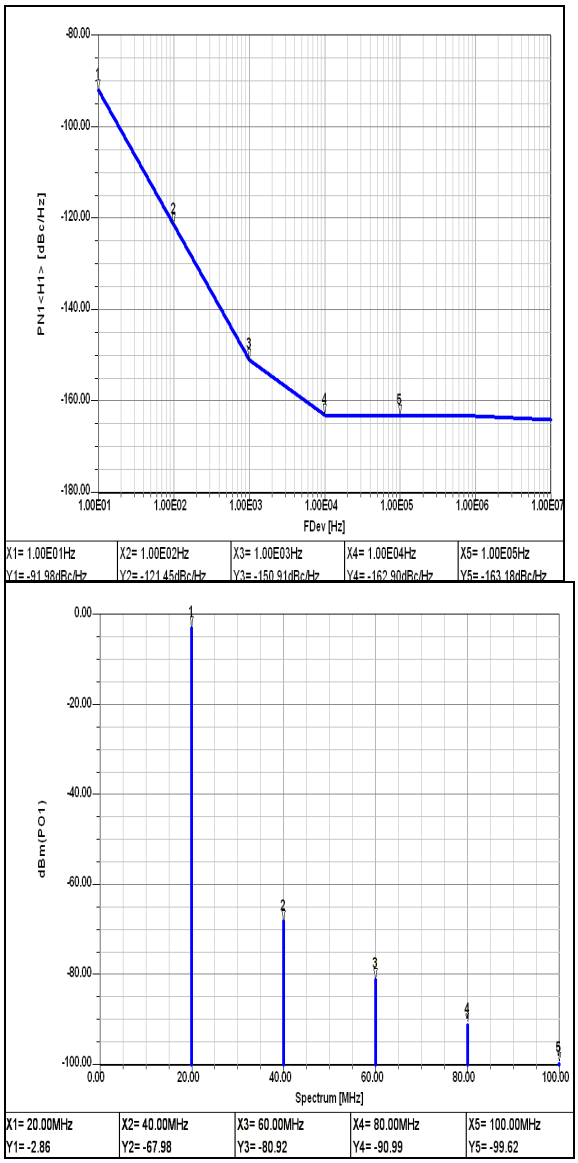


Figure 37: a) Simulated phase noise of 20MHz Butler oscillator and, b) simulated output response

Few more examples studied are presented here from reference 21.

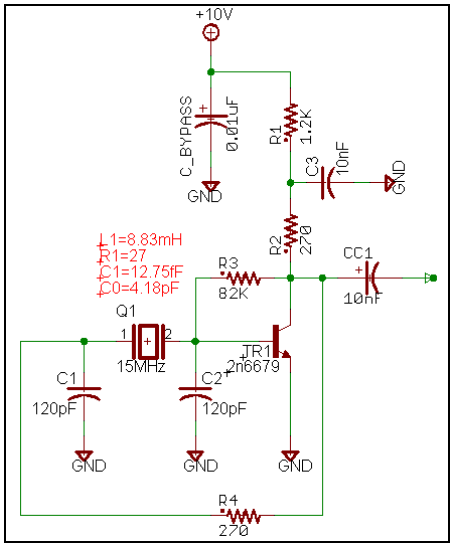


Figure 38: 15MHz Pierce Oscillator.

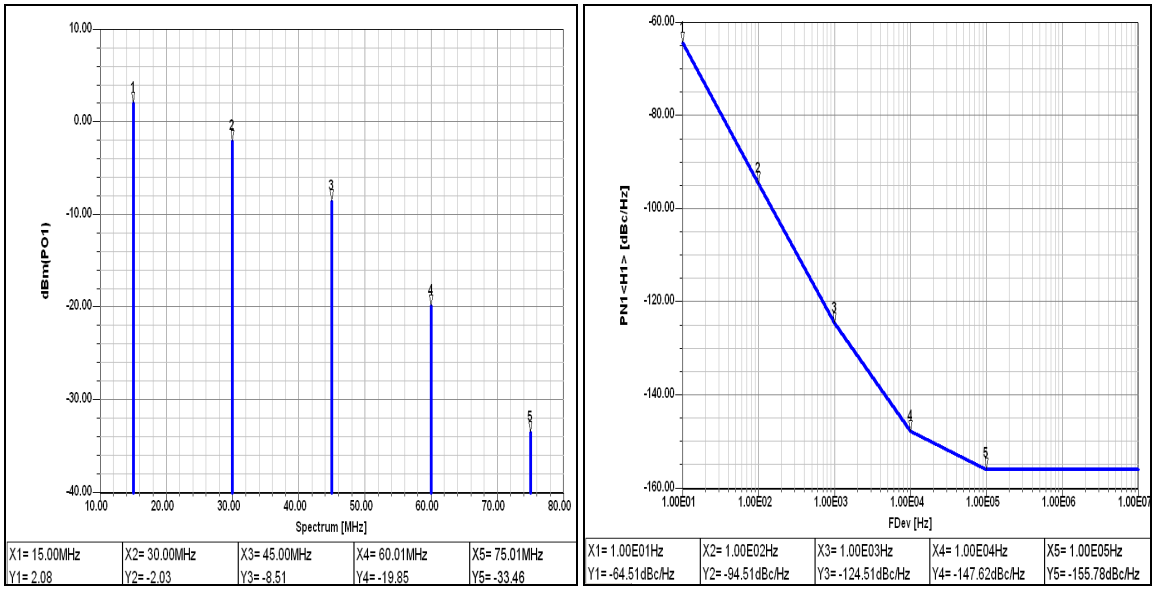


Figure 39: 15MHz Pierce Oscillator (a) Output Response, (b) Phase noise

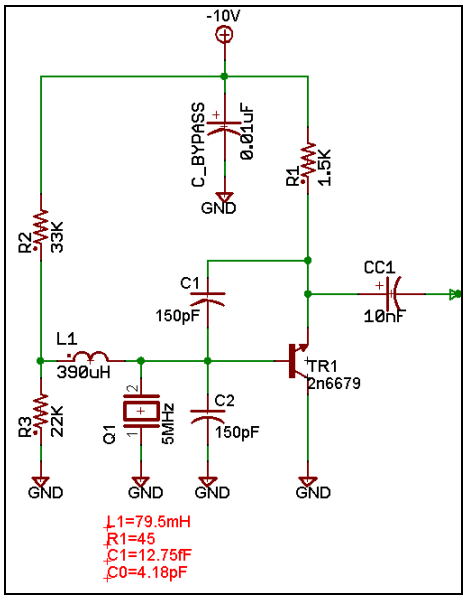
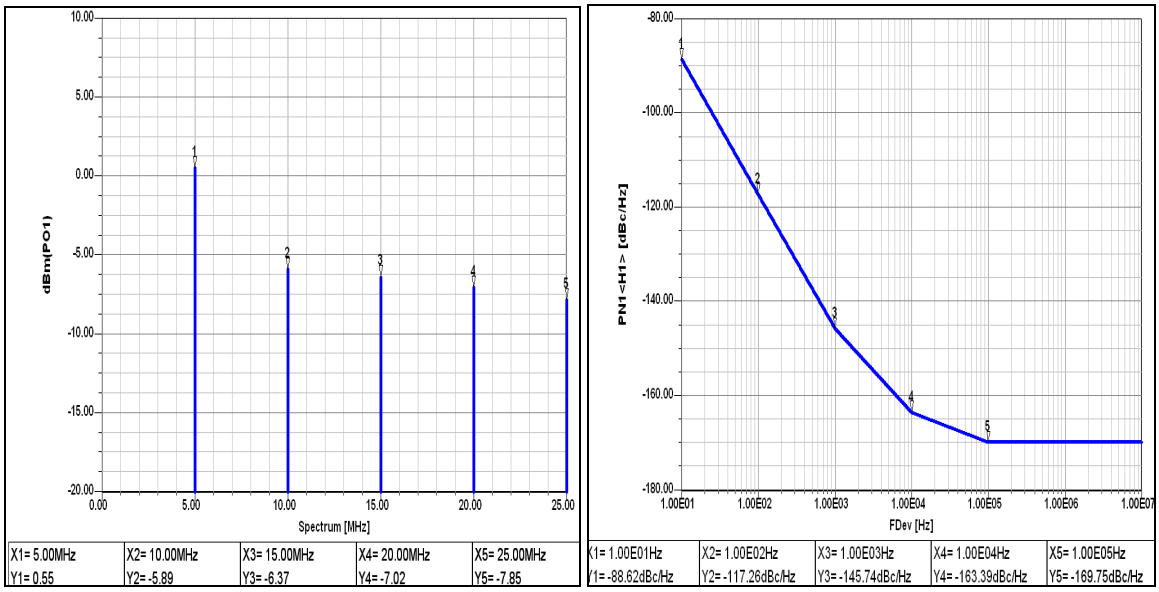


Figure 40: 5MHz Colpitts oscillator.



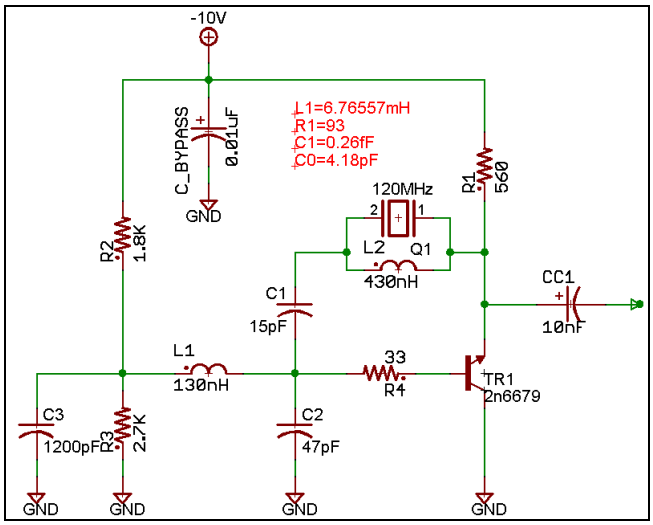
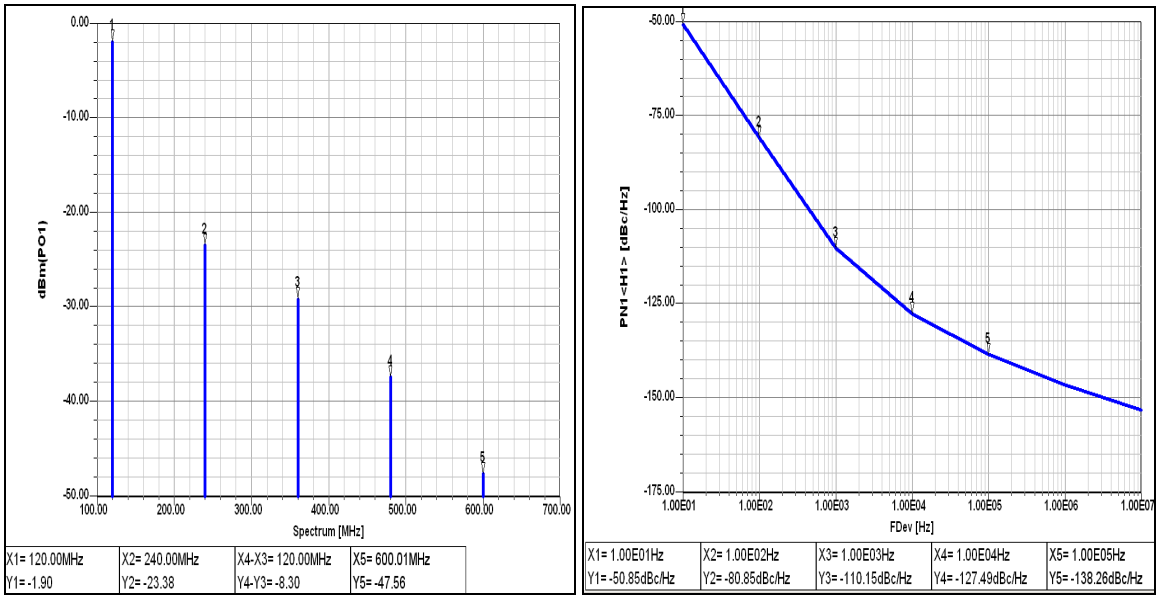


Figure 42: 120MHz Butler oscillator (Emitter output).



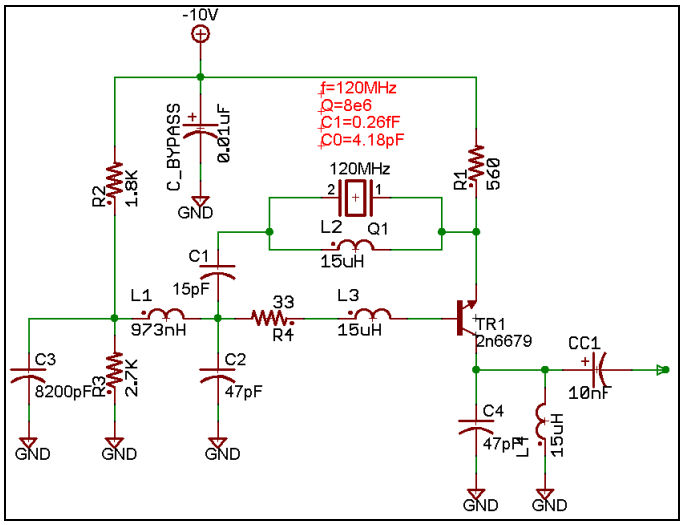
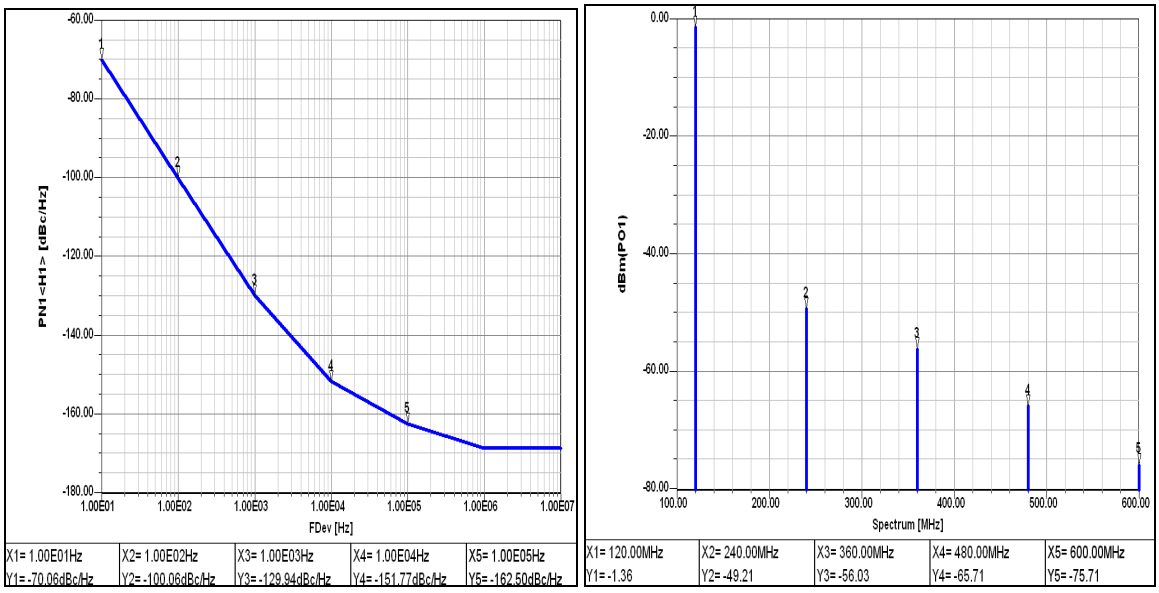


Figure 44: 120MHz Butler oscillator output at the collector.



This section should be used only as guideline aids to selecting the configuration type for the oscillator once the design specifications are decided. Crystal oscillators above 100MHz can be easily built, but it is often preferable to use a lower frequency oscillator followed by the frequency multiplier. This arrangement is often more practical in production environment. There are many different types of oscillators apart from the ones listed here that offer excellent performance in certain areas. These guidelines are for few commonly used simple to design configurations that still offers good performance. The principal difference between the Pierce and Colpitts configuration is the choice of signal ground. One must note that since the only change is the choice of signal ground, the negative resistance equation that governs the Colpitts oscillator are also valid for small signals will also be valid for Pierce oscillator. This means that the small signal gain requirements are the same and the circuit will oscillate if, $gmXc_1Xc_2 \rangle R_E$, where R_E is the real part of the series impedance across the crystal, Xc_1Xc_2 are the impedance of the capacitance in the voltage divider and gm is the transconductance for the transistor. Even though this is true still the performance for both of them will be quite different due to different limiting action, occurring under the large signal conditions. All these configurations can be optimized to get more-or less the same phase noise at the cost of certain parameters. Note: Overtone crystals are not a good choice when large frequency deviation is required. The pullability of crystals (change in frequency) is inversely proportional to the square of the overtone number, so as the higher overtone crystals are used the pullability available reduces.

$$\frac{C_N}{N^2} = \frac{2*\Delta f\left(C_0 - C_L\right)}{f*10^6} \Rightarrow \frac{1}{N^2} \propto \Delta f$$

Summarizing the general advantages and disadvantages of the various configurations of oscillator:

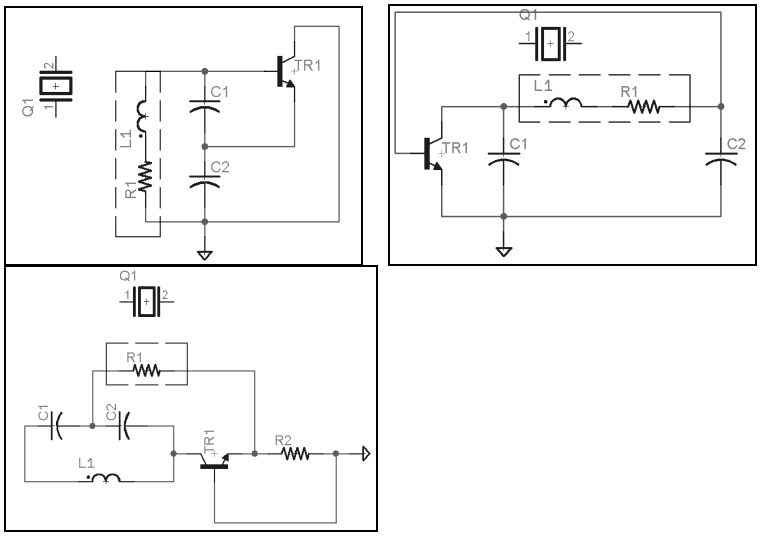


Figure 46a: Colpitts Configuration Figure 46b: Pierce Configuration Figure 46c: Butler Configuration

Colpitts oscillator:
This configuration is designed to take the output from the emitter and the collector is tied directly to the supply voltage. This design is fairly simple and the performance is moderate to good. As there is no collector resistor, the limiting is due to the cutoff in transistor. With crystal, this design can be used for very small frequencies and needs modifications in it as the frequency increases. The Colpitts configuration works very well for low aging and good performance oscillators upto 50 MHz. The amplifier in Colpitts is an emitter-follower. Feedback is provided via a tapped capacitor voltage divider (C1 and C2). The cost to build these oscillators is less and so is the number of components used in the circuit, typically less than ten components will be used.

Semi-isolated Colpitts oscillator (Output from Collector):
This configuration is designed to take the output from the collector. More power is available at the output from collector than the power extracted from the resonator. The miller capacitance limits the operation of these configurations at high frequencies. But the advantage of such a configuration is the impedance in the collector branch can be tuned to its higher harmonics. This means for high frequency applications a frequency multiplication action from such configuration should be used with the collector tank tuned to its higher harmonic. The isolation from load to the oscillator circuit is also much better when the output is a harmonic of the oscillator frequency. The Coupling capacitor loads the circuit and more power is extracted. But capacitive load will reduce the operating Q of the circuit and the transistor may go into saturation if the load is too high.

Semi-isolated Configuration (Cascode Configuration, Output from Collector):
The output of the semi-isolated colpitts configuration can be dc coupled into a common base amplifier in a cascode arrangement. This modification gives excellent isolation to the load and allows for a much larger collector load in the second transistor. These circuits are slightly more complex to design and manufacture. Also we need a higher power supply requirements to properly bias the amplifier and thus have more power consumption. This kind of design is more preferred at the higher frequency range than the traditional Colpitts. As the common base amplifier is used in this configuration the degradation of Q, caused by the low impedance of emitter terminal of transistor, will be less. The crystal is placed such that there is current flow through the resonator that makes the crystal to act as a filter there by providing a better noise-floor.

Driscoll oscillator:
Driscoll is a more complex crystal oscillator with excellent performance characteristics. It is a cascaded stage of inverting common emitter amplifier along with the phase shifter. Without the crystal, this circuit is more effectively like a Pierce oscillator or the old Vackar VFO. The Driscoll oscillator basically turns the semi-isolated cascode configuration around and uses the common emitter (CE) oscillator with the crystal connected between the emitter and ground. This results

in degradation of Q of the crystal, which makes contact with the collector terminal of the transistor that has low impedance due to the input stage of CE amplifier.

Semi-isolated Colpitts oscillator (Output from Collector):
Another modified version of semi-isolated Colpitts oscillator is one in which the output is extracted from the resonator. The principal disadvantage of this circuit is low power at the output. These circuits are terminated by a cascode stage at the output. By extracting the resonator power through crystal, the crystal acts as a very narrowband filter on noise generated by the oscillator stage. The common base stage offers a very low impedance and the Q degradation will be very small. The ratio of crystal power to oscillator output power is equal to ratio of crystal resistance to common base input. As the output is from the resonator itself the harmonic contents are suppressed more in this configuration.

Pierce configuration:
The Pierce oscillator is capable for a good performance at high frequencies. Note that if the emitter is grounded for the Colpitts, the configuration changes to Pierce. The important difference of biasing arrangement in Pierce oscillator increases the effective resistance of the crystal thus reducing its Q and decreasing the loop gain. The impedance at the collector may cause transistor saturation. If optimized for low aging then the crystal power may also become excessive. There is some tendency of spurs at high frequency. The package inductance at the base pin of the transistor will generate the undesired resonance at very high frequency. For example in 10MHz oscillator a response may also be present at 5GHz.

Modified Pierce Configuration (Output from resonator):
In the modified Pierce oscillator configuration the crystal operates in a series resonant mode, so we can tune out the crystal motional capacitance of the crystal giving more linearity and reducing the out-of-band noise. In series mode the current in the crystal will be much less than the available power of the oscillator. This generates the need for a buffer amplifier at the output to achieve the power requirement. Both these parameters, less current at the output and the buffer amplifier increase the far-out phase noise. But the crystal acts as a filter itself for the close-in noise.

Butler configuration:
The Butler oscillator gives good performance for frequencies from 10MHz to VHF. This is because the collector to base capacitor is effectively grounded. Butler oscillators are quite susceptible to spurious resonances. The amplifier is an emitter follower. The output of the common butler oscillator is taken from the ac grounded base of the oscillator. When a high frequency operation is desired the tank circuit is used in collector, which is used as the output terminal. To operate on the overtone frequency the tank circuit resonance is tune changed. The advantage of the butler oscillator is that a small voltage exists across the crystal, reducing the stress on the crystal.

Some Validated Circuit:
(Left Blank Intentionally as Separator)

Schematic from figure 18 was built and validated for truth. The overall built circuit was as follows.

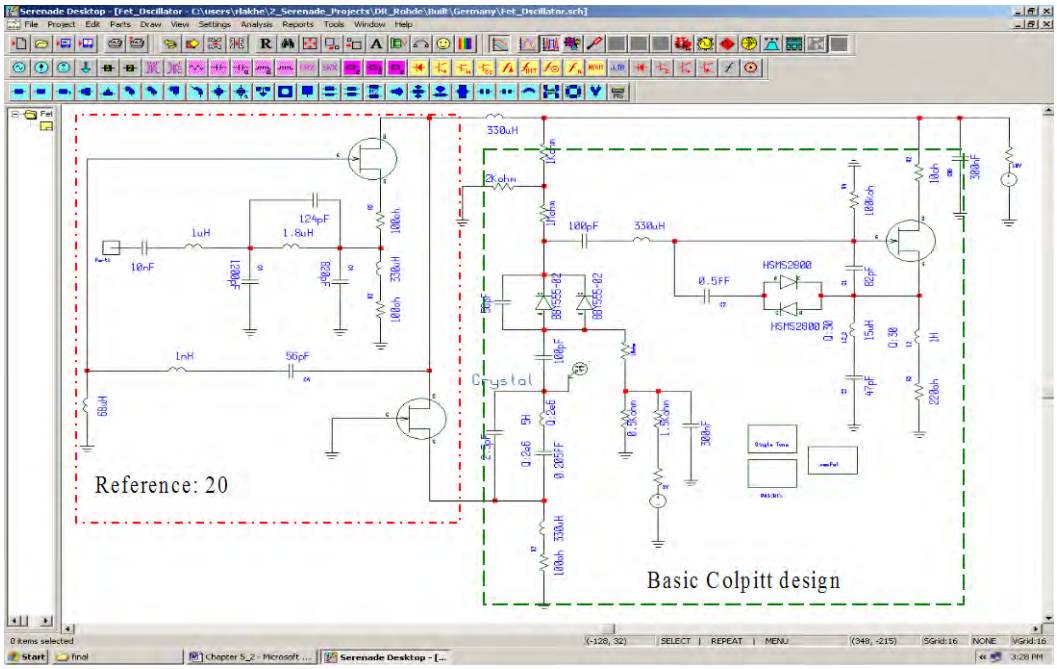


Figure 47: 5MHz Colpitts oscillator with output from resonator.

In the normal Colpitts oscillator the output is taken from the resonator, reference 20 and then passed through an amplifier and filter. When the output is taken from the resonator the output is less compared to the output we can get from collector/ drain or the emitter/source of the active device. Hence we need an amplifier at the output stage, but this results in slightly high harmonic content, so a filter is used to suppress it. The simulated response for the overall circuit is as shown below in figure 48. Figure 49 shows the measured response of the circuit.

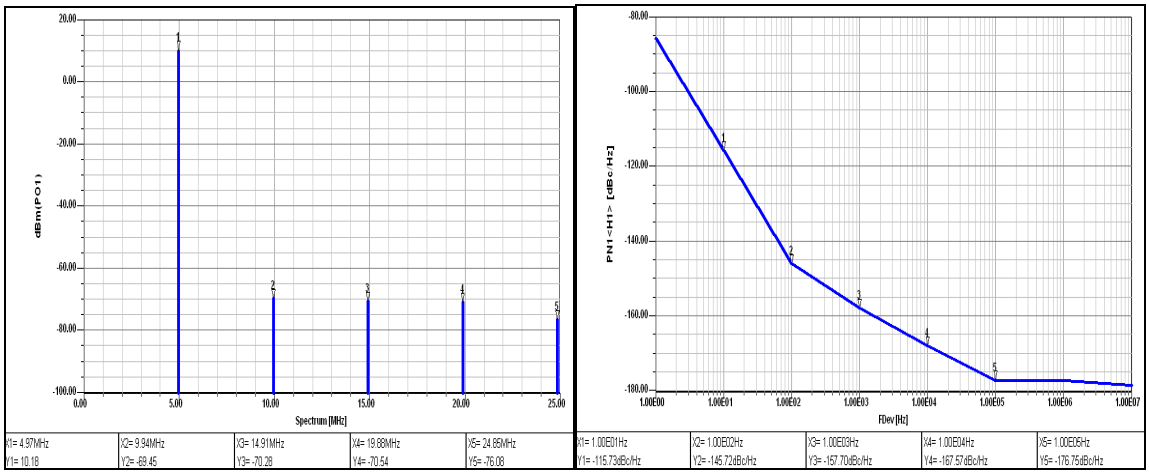


Figure 48: (a) 5MHz Colpitts oscillator output with harmonic suppression around –80dBc/Hz (b) Phase noise of the 5MHz Colpitts oscillator.

To validate the design approach, a commercial 155.6 MHz VCXO was used as an example to apply the concept of mode-feedback, and mode-coupling mechanism. The promising alternative for high performance VCXO at 155.6 MHz is overtone mode, which is similar in concept to a harmonic, with the exception that crystal oscillation overtones are not exact integer multiples of the fundamental. The new approach includes dynamic noise filtering, mode-feedback, noise-feedback, and mode coupling for optimum group delay to enhance the loaded Q and suppress mode-jumping phenomena (especially when the crystal resonates at higher odd-order overtone modes).

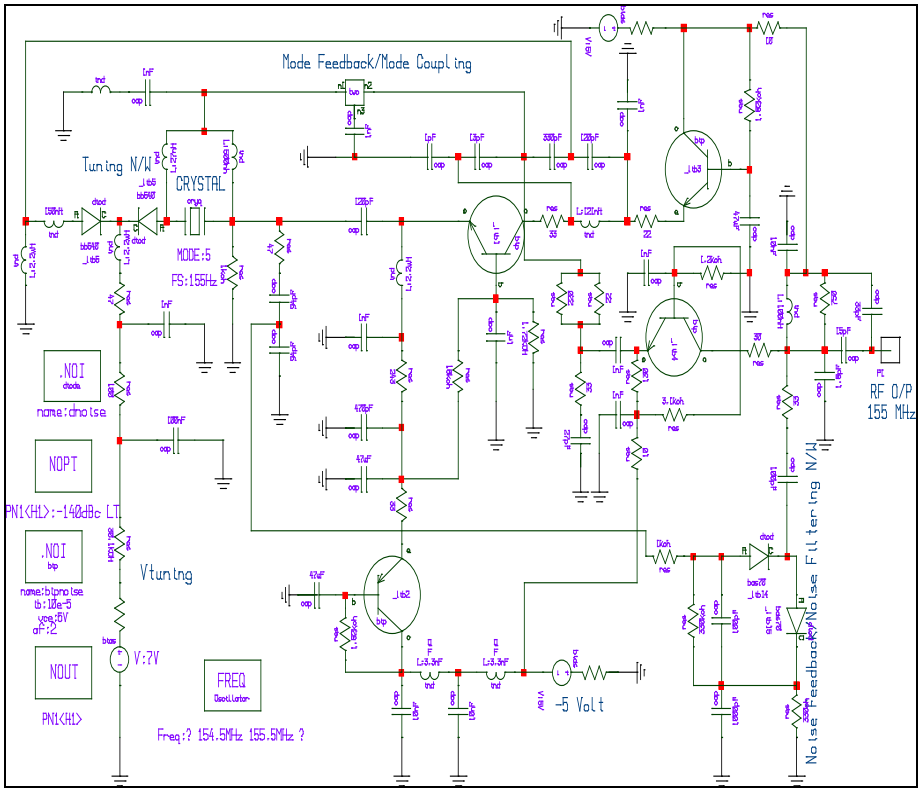


Figure 50: 155.6 MHz Mode-Feedback 5th overtone VCXO (Patent Pending)

Figure (50) shows the 5th overtone 155 MHz VCXO circuits in which higher order mode is coupled through output path and feedback to the point where resonator impedance shows steep change of phases, thereby, maximization of group delay [12]-[19]. Additional improvement in the phase noise is achieved by dynamically optimizing noise-feedback and mode-coupling mechanism. The dynamic noise-feedback is an effective method to reduce the 1/*f* noise. By introducing an additional low frequency negative feedback loop, the close-in noise is reduced by approximately 10-15 dB in the flicker region. A mode-feedback and noise filtering offers significant improvement in phase noise performances (-139

dBc/Hz @ 100Hz offset for 155.6 MHz carrier frequency) and was validated using cad software.

Figure (51) shows the measured phase noise plot, which closely agree with the simulated result for both approaches (with and without mode-feedback). At lower offset (1Hz), improvement in phase noise performance is limited due to the influence 1/*f* noise, which can be optimized by selecting transistor that has low value of 1/*f* noise.

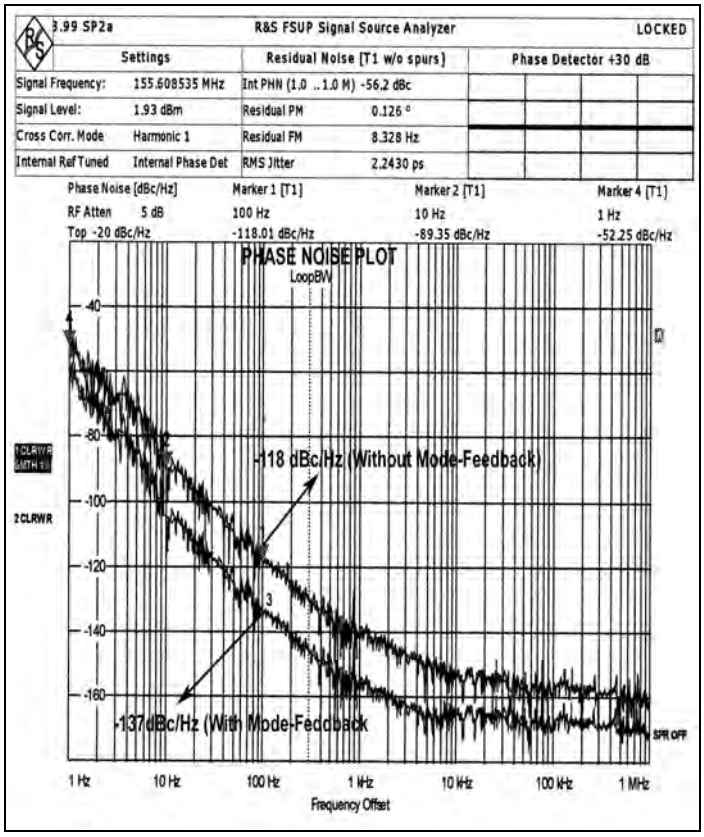


Figure 51: Measured phase noise plots for 155.6 MHz 5th overtone VCXOs

References:

There will be up to 50 other references

U. L. Rohde, Microwave and Wireless Synthesizers, Theory and Design, Wiley, New York, 1997 pp. 236-277.

John R. Vig, A Tutorial- Quartz crystal resonators and oscillators for Frequency Control and Timing Applications,November 2008, J.Vig@IEEE.org

U.L.Rohde and A.K.Poddar, *Mode selection and mode-feedback techniques optimizes VCXO performances*, IEEE Sarnoff symposium, Princeton, NJ, USA, April 28-April 30, 2008.
U.L.Rohde and Ajay K. Poddar, Dynamic noise-feedback and mode-coupling mechanism silences the VCXOs phase noise,
Ulrich L. Rohde, Ajay K. Poddar, & Georg Böck, The design of modern microwave oscillators for wireless applications, theory and optimization, Wiley, New York, 1997.
Ansoft Serenade.
U. L. Rohde, George D. Vendelin and Anthony M. Pavio, *Microwave circuit design using linear and nonlinear techniques*, Wiley, New York, 2005 pp. 175.
Parzen et. Al
M.E.Frerking
To be filled
To be filled
U. L. Rohde and A. K. Poddar, "Wideband voltage controlled oscillators employing evanescent mode coupled resonators," *US Patent No*. 71803812, Feb 2007.
U. L. Rohde, A. K. Poddar, and R. Rebel," Integrated Low Noise Microwave Wideband Push- Push VCO", *US Patent No*. 7,088189, Aug 2006.
U. L. Rohde and A. K. Poddar," User-Definable Thermal Drift Voltage Controlled Oscillator", US Patent No.7, 265,642 B2, Sept 4, 2007.
U. L. Rohde and A. K. Poddar," Low Thermal Drift Tunable Frequency Voltage Controlled Oscillatory", US Patent No.7262670 B2, Aug 28, 2007.
U. L. Rohde and A. K. Poddar," Tunable Oscillator", US Patent No.7, 292,113, Nov. 6, 2007.
U. L. Rohde and A. K. Poddar," Tunable Frequency, Low Phase Noise and Low Thermal Drift Oscillator", *US Patent No.7196591*, March 2007.
U. L. Rohde and A. K. Poddar," Multi-Octave Band Tunable Coupled-Resonator Oscillator", *US Patent No.* 292,113, Nov. 6, 2007.
U. L. Rohde and A. K. Poddar," Low Noise, Hybrid Tuned Wideband Voltage Controlled Oscillator", *US Patent No.* 7,365,612, April 29, 2008.
U.L.Rohde, *Crystal Oscillator Provides low noise*, Electronic design magazine, pp21. Oct.11, 1975.

Randall W. Rhea, Oscillator design and computer simulation, SciTech publishing inc., NJ, Second edition 2006 Chapter 11.