COVER FEATURE
INVITED PAPER

Editor's Note: Exactly one decade ago, Alexander Chenakin wrote about the state of the synthesizer market and future directions in Microwave Journal. *The article has been referenced by many authors that followed and most of his projections were proven correct over time. Now he is back with another look at the current design trends in synthesizers and more future directions for another decade of inspiration.*

Frequency Synthesis: Current Status and Future Projections

Alexander Chenakin
Micro Lambda Wireless Inc., Fremont, Calif.

There is persistent pressure on the RF/microwave industry to deliver higher performance, higher functionality, smaller-size, lower-power-consumption and lower cost synthesizers.[1-18] Although all synthesizers exhibit significant differences as a result of specific applications, they share basic fundamental design objectives as depicted in ***Figure 1***. The ideal synthesizer should preferably be broadband with fine frequency resolution that allows addressing a larger number of potential applications. Aside from frequency coverage and resolution, phase noise and spurs are critical parameters that impose the ultimate limit in the system's ability to resolve signals of small amplitude. Another key parameter that impacts overall system performance is frequency switching speed. The time spent by the synthesizer transitioning between frequencies becomes increasingly valuable since it cannot be used for data processing. Modern synthesizers tend to be faster due to the ongoing increase in the data rates of RF/microwave systems. Another challenge is size and cost reduction. These requirements—wide frequency coverage, small step size, fast switching speed, adequate spectral purity, small size and low cost—are the key drivers in the development of modern frequency synthesizers.

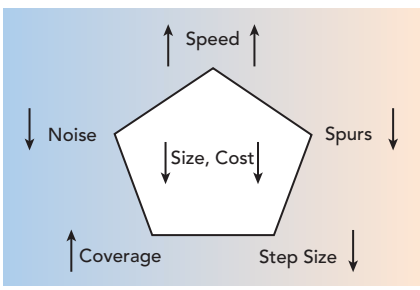


Fig. 1 Synthesizer design challenges.

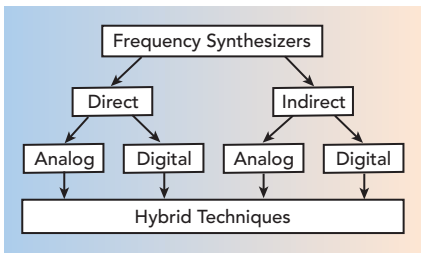


Fig. 2 Frequency synthesizer classes.

ARCHITECTURES

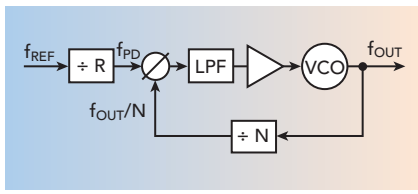
Synthesizer characteristics depend heavily on a particular architecture, which can be classified into a few main groups as indicated in ***Figure 2***. Direct architectures are intended to create the output signal directly from available reference signals either by manipulating and combining them in the frequency domain (direct analog synthesis) or by constructing the output waveform in the time domain (direct digital synthesis). The indirect methods assume that the output signal is regenerated inside the synthesizer in such a manner that the output frequency relates (e.g., is phase-locked) to the input reference signal. Similarly, indirect synthesis can be accomplished with analog and digital techniques. A practical synthesizer, however, is usually a hybrid design that combines various techniques to take advantage of the best aspects of each.

INDIRECT SYNTHESIS

For decades, an indirect phase-locked loop (PLL) synthesizer was

(and still remains) the most common and most popular technique. A generic single loop PLL (see ***Figure 3***) includes a tunable voltage-controlled oscillator (VCO) that generates a signal in a desired frequency range. This signal is fed back to a phase detector through a frequency divider with a variable frequency division ratio N. The other input to the phase detector is a reference signal divided down to a desirable step size. The phase detector compares the signals at both inputs and generates an error voltage, which following filtering (and optional amplification) slews the VCO until it acquires the lock frequency given by $f_{OUT} = Nf_{PD}$, where f_{PD} is the comparison frequency at the phase detector input. Thus, frequency tuning is achieved in discrete frequency steps equal to f_{PD} by changing the division coefficient N.

This simple PLL synthesizer exhibits various limitations and tradeoffs. The main impact on synthesizer performance is caused by the large division ratios required to provide a high frequency output with a fine resolution. Note that any noise generated by PLL components is degraded at a 20logN rate, where N is the division ratio. In conventional integer-N PLLs operating with small step sizes, the division ratio is large because the step size must be equal to the comparison frequency at the phase detector. As a result, significant phase noise degradation occurs. Furthermore, the synthesizer switching speed is a function of its loop bandwidth and, therefore, is limited by the phase detector comparison frequency. Increasing the loop bandwidth may lead to higher reference spurs due to insufficient loop filter rejection or even loop instability. Thus, this simple single loop architecture suffers from mutually exclusive design goals. It is usually utilized in non-demanding applications or when low cost is the major concern.



▲ **Fig. 3 Single loop PLL synthesizer.**

Fractional-N Synthesizer

Fractional-N synthesizers break this coupling between frequency resolution and other characteristics by using fractional division ratios, allowing a higher comparison frequency for a given step size. Fractional ratios are possible by alternating two (or more) division ratios (let's say, N and N+1) and averaging the output frequency over a certain period of time. Another way to look at this process is to calculate the number of pulses delivered by such a complex divider for a given time interval. Obviously, the average division coefficient will be between N and N+1 depending on how many pulses are processed by each individual divider. The biggest concern associated with this scheme is that the instant frequency at the fractional-N divider output is not constant. An abrupt change in the division coefficient leads to a phase discontinuity that produces a voltage spike at the phase detector output. Since the frequency division change occurs periodically at the same rate, it appears as discrete spurs in the synthesizer's output spectrum. Suppression of the resulting spurs requires that the PLL filter bandwidth must be sufficiently small, which may affect phase noise and speed performance.

There are many techniques to reduce fractional-N spurs.[19-21] In general, this can be accomplished by adding or subtracting a voltage at the phase detector output during the frequency division change. Another method is based on using a multi-modulus divider that allows a larger number of division coefficients. In this case, we should expect a larger number of spurs of smaller amplitude. The multi-modulus divider is often accompanied by a delta-sigma modulator that allows randomizing frequency spurs and pushing them towards higher offset frequencies where they can be filtered by the loop filter. In spite of various improvements, the main disadvantage of the fractional-N technique is the excessive spurious levels produced by phase errors inherent in the fractional division mechanism.

A clever method to reduce fractional spurs is to utilize a variable

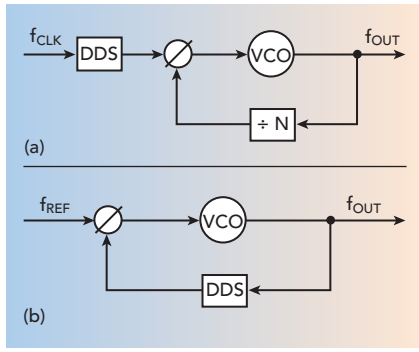


Fig. 4 Using a DDS as a fine resolution high frequency reference (a) or fractional divider (b) within a PLL synthesizer.

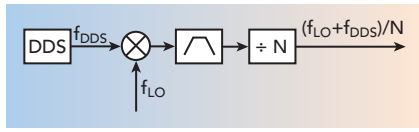


Fig. 5 Up-converting and dividing a DDS signal.

reference. The technique is based on the fact that spur location in a fractional-N synthesizer is a function of its particular division ratio and output frequency. Therefore, for a given output frequency one can move (and then filter out) an undesired spur by changing the reference frequency and corresponding division ratio. This involves thorough frequency planning and also requires an additional frequency synthesizer (to be used as a reference). Furthermore, although the division ratio is reduced, it can still be high enough to affect PLL performance.

Direct Digital Synthesis (DDS) Within a PLL Synthesizer

The DDS is another effective solution to provide a very fine frequency resolution without a common penalty of the phase detector comparison frequency reduction. The DDS can serve as a fine resolution, high frequency reference or be employed as a fractional divider as illustrated in ***Figure 4***. While a DDS provides excellent frequency resolution, its spurious levels are usually quite high. Moreover, the spurs further degrade because of the PLL multiplication mechanism. Although the two schemes in Figure 4 look different, they both affect DDS spurs in the same manner. In both cases, the overall loop division coefficient is defined by the ratio between the

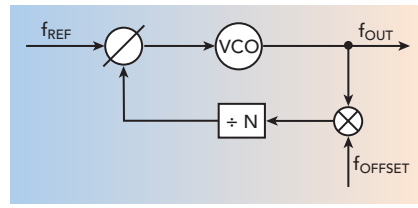


Fig. 6 Frequency offsetting improves PLL performance.

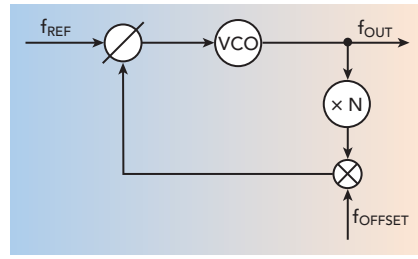


Fig. 7 Inserting a multiplier into the PLL feedback path.

VCO output and phase detector comparison frequencies. The DDS spurs can be reduced by utilizing many techniques, for example, using a variable clock (as described above for the fractional-N synthesizers) or up-converting and further dividing down the DDS signal as illustrated in ***Figure 5***. Note that the up-converted relative DDS bandwidth is reduced and often needs further extending as required by a particular frequency plan. This can be achieved through various methods; for example, by using variable (versus fixed) frequency division coefficients.

Frequency Offset and Multiplication Within a PLL Synthesizer

The synthesizer's main characteristics can be drastically improved using frequency conversion (mixing) within the synthesizer feedback path as shown in ***Figure 6***. The idea is to convert the VCO output to a much lower frequency with the aid of a mixer and an offset frequency source. In certain scenarios (e.g., when the operating frequency range is narrow) it is possible to eliminate the feedback frequency divider completely. In this case, the loop division coefficient equals one, and no phase noise degradation occurs. Moreover, one can further reduce PLL component residual noise impact by inserting a frequency multiplier into the feedback path instead of a divider as depicted in ***Figure 7***.

Multi-Loop Synthesizer Schemes

The main disadvantage of the simple frequency offset schemes is limited frequency coverage. Widening the output frequency bandwidth for a fixed offset frequency leads to a higher IF at the mixer output. This requires a divider with a larger division coefficient, thus defeating the idea of this method. The offset frequency signal should preferably be as close as possible to the RF output frequency in order to keep the division ratio at a minimum. This can be accomplished in multi-loop schemes by utilizing a wideband offset signal (see ***Figure 8***).

Use of a Mixer Chain in the Feedback Loop

A clever solution is to utilize a chain of mixers within PLL feedback path as illustrated in ***Figure 9***. Individual offset signals can be obtained from a common high frequency variable reference using dividers and/or multipliers. In this case mixer intermodulation products coincide with phase detector comparison frequency harmonics and thus can be easily filtered out by a loop filter.[22]

DIRECT SYNTHESIS

Direct Analog Synthesizer

Direct analog synthesis is a totally different ball game. As the name suggests, the desired signal is created directly (i.e., without regeneration) by mixing base frequencies followed by switched filters, as conceptually shown in ***Figure 10***. The base frequencies are normally obtained from a common reference by frequency multiplication, division and/or mixing. The key advantage of the direct analog technique is extremely fast switching speed, ranging from micro- to nanoseconds. Since direct analog synthesis assumes no closed loops, switching speed is limited only by propagation delays of the switches and their control circuits as well as filter settling.

Another distinct advantage is the ability to generate low phase noise due to use of components with negligibly low residual noise. Phase noise depends mainly on the noise of the available fixed-frequency sources and can potentially be very low. The main disadvantage is limited frequency coverage and step size. The number of output frequencies can be increased by using a higher number of base frequencies and/or mixer stages, however, this rapidly increases the design complexity and overall component count.

Another serious problem is the large amount of mixing products that must be filtered. These include the undesired mixer sideband, LO leakage and intermodulation prod-

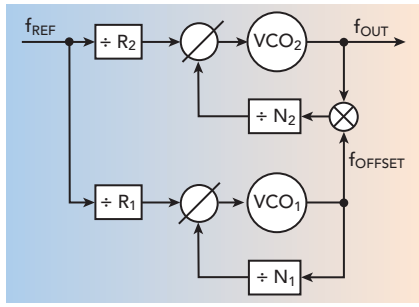


Fig. 8 Multi-loop synthesizer.

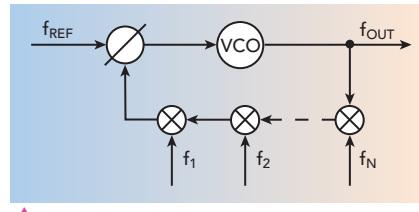


Fig. 9 Mixer chain in the PLL feedback path.

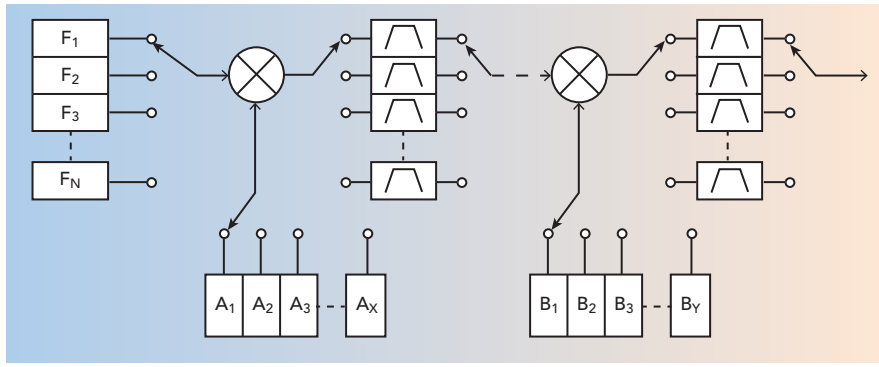
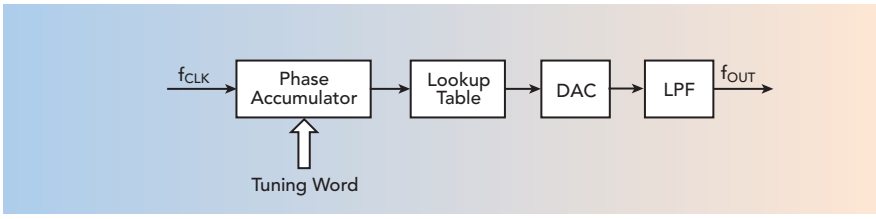


Fig. 10 Direct analog synthesizer.

ucts. Depending on a particular frequency plan, filtering close-in spurs can be a challenging task. This is a non-trivial consideration requiring certain design effort and careful frequency planning. Although a large variety of mixing and filtering schemes are possible, they tend to be hardware intensive if a small frequency step and wide coverage are required. Therefore, while direct analog synthesis offers excellent tuning speed and phase noise characteristics, its usage is limited to applications where fairly high cost can be tolerated.

Direct Digital Synthesizer

In contrast to traditional concepts, direct digital synthesizers utilize digital signal processing to construct an output signal waveform in the time domain piece-by-piece from a reference clock frequency. Initially a digital representation of a desired signal is created using a phase accumulator and lookup table (see ***Figure 11***). Then it is reconstructed with a digital-to-analog converter (DAC) to create a sinusoid or any other desired shape. The waveform construction process is completed with a lowpass filter to remove unwanted spurious components. This process is extremely fast, limited mainly by the speed of the digital control logic. This results in very high switching speeds, comparable with direct analog schemes. The DDS also provides reasonably low phase noise even showing an improvement (limited by its residual noise floor) over the phase noise of the clock source itself. The most valuable DDS feature, however, is its exceptionally fine frequency resolution determined by the length of the phase accumulator; sub-Hz levels are easily achieved.



▲ Fig. 11 Direct digital synthesizer.

The main disadvantage is limited usable bandwidth. While DDS starts working from nearly DC, its highest frequency is limited by the Nyquist criteria to one half of the clock frequency. Working in higher Nyquist zones is possible, however, performance degrades very quickly. Another serious problem is a relatively high spurious content due to a number of factors inherent in the DDS technique, such as bit truncation, quantization and DAC conversion errors.

DDSs are available as specialized fully-integrated chips or can be built using separate field programmable gate array (FPGA) and DAC ICs. The latter allows constraining the digital part within FPGA, thus, isolating its EMI-induced spurs. Today's FPGAs have sufficient capacity to build quite complex multicore phase accumulators and lookup tables with negligible spur levels due to bit truncation. As a result, the major spur sources are normally on the DAC side due to its nonlinearities and quantization noise. DAC-free solutions are also possible (for example, using digital-to-time conversion)[23], although, they are currently not common.

Until recently, the DDS technique was rarely used alone at microwave frequencies. However, the rapid development of high frequency ICs enables DDSs working directly at microwave frequencies with quite impressive characteristics such as microhertz resolution, nanoseconds-range switching speed and built-in modulation. The extension of DDS usable bandwidth (together with its spur content reduction) is the key improvement required by the industry.

EVOLUTION AND FUTURE PROJECTIONS

A synthesizer is traditionally expected to generate a continuous wave signal within its operating frequency range. Its amplitude may vary with frequency within

certain limits. However, newer designs bring more functionality such as amplitude leveling and control. The output level can be calibrated and controlled using either open-loop (lookup table) or more sophisticated close-loop automatic level control (ALC) schemes. Furthermore, these days the industry demands more complex waveforms ranging from traditional analog modulation (amplitude, frequency, phase and pulse) to complex vector formats such as IQ modulation. These modulation capabilities together with amplitude control and harmonic rejection can now be built not only in bulky test and measurement signal generator boxes, but also in smaller form factor modules. Key performance characteristics (such as phase noise, spurs and switching speed) are approaching those of dedicated test and measurement signal generator solutions as well.

With respect to phase noise performance, synthesizer designers rely primarily on 100 MHz ovenized crystal oscillator (OCXO) technology. Today's commercial OCXOs achieve -170 to -176 dBc/Hz (and better) at 10 kHz offset and 100 MHz output. This can potentially translate to -130 or -136 dBc/Hz at 10 GHz assuming the synthesizer circuitry is "ideal." Although nothing is ideal, all current developments are striving for ideality. At low frequency offsets (100 Hz and below), a 10 MHz OCXO performs better. Furthermore, its short-term stability is also better compared to a 100 MHz oscillator. Hence, a synthesizer design usually provides the capability to lock its output to a 10 MHz reference. Similarly, high frequency oscillators (such as SAWs and DROs) perform better at high frequency offsets such as 100 kHz and above.[24-29] A combined reference source containing several oscillators locked to each other can be used to achieve the lowest phase noise profile at any frequency offset. Further improvements are possible through the use of higher-Q resonators such as sapphire-loaded cavities or optical methods.[30-33]

CONCLUSIONS

Overall, the indirect, VCO-based PLL synthesizer remains the most popular approach at the moment. Further improvements are expected through reduction of the PLL residual noise floor in order to support megahertz-range loop bandwidths. Fast switching speed (to several microseconds) and low phase noise (around -130 dBc/Hz at 10 kHz offset and 10 GHz output) are common goals for today's designs and those of the near future. Small form factor, extended functionality (such as built-in modulation and amplitude control) and low cost are design targets required by the industry.

The most exciting future developments, however, are likely to be associated with DDS technology, which has tremendous potential for growth. Much of the progress will be brought by extension of DDS usable bandwidth and reduction of its spurious content. Frequency multiplication and/or up-conversion is possible to bring available frequency bandwidth to mmWave frequencies and higher (although the native DDS bandwidth will constantly grow). At some point, direct synthesis is expected to compete with and eventually replace indirect designs by offering amazingly fast, nanosecond-range tuning speed as well as complex output waveforms.

Longer term major breakthroughs are expected in the design and operation of the reference utilizing other physical principles or materials. For example, phase noise around -170 dBc/Hz at 10 kHz offset and 10 GHz output for a sapphire-resonator-based oscillator has been reported.[34] These expectations will dramatically change conceptual approaches for building new synthesizers or even the whole way of thinking about the problem. What performance can be eventually achieved? Only the future will tell. A lot of amazing developments are expected in the coming decades. ■

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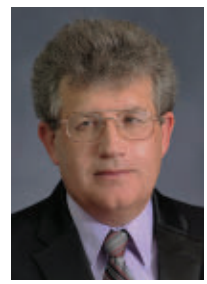

Alexander Chenakin *is vice president of Advanced Technologies at Micro Lambda Wireless Inc. in Fremont, California, where he oversees the development of advanced signal generator products. Dr. Chenakin previously held a range of technical and executive positions at Phase Matrix, National Instruments, Anritsu and other companies. He is well recognized in the field of frequency synthesis and is referred to as the inventor of QuickSyn technology. In 2009, he received ARMMS RF & Microwave Society's best contribution award for his work on fast switching frequency synthesizers.*

Dr. Chenakin's professional achievements have been widely presented in trade publications and international conferences. He has written more than 40 technical articles and holds two U.S. patents. In addition, Dr. Chenakin is the author of an Artech House published textbook about frequency synthesizers. He is a senior IEEE member and has been an invited speaker at several IEEE-sponsored events.