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Simple SDR Receiver

Looking for some hardware to learn about SDR?
This project may be just what you need to explore this hot topic!

This article describes the design and the theory of operation of an HF radio receiver operating in the 3.5 to 18 MHz range. The receiver architecture is based on software defined radio techniques and incorporates a Cypress PSoC CY8C3866 device that contains both analog and digital circuits, thus decreasing the receiver's component count. This part is far more than just a microcomputer; it also contains software configurable analog and digital peripherals on a single chip. Cypress calls the family a PSoC in reference to it being a programmable embedded system-on-chip. The newest series of parts, which Cypress calls the PSoC 3 family, contains a 67 MHz 8051 class microcomputer, an analog to digital converter fast enough and with enough resolution for an SDR receiver, and other valuable functions that are desirable in a receiver design.

The receiver should be used for casual, conversational listening; it is not intended as a higher performance receiver for DX use. It was designed to use a minimum number of components, to be physically small and easy to operate. An LCD and controls to select the frequency and modes of operations were considered, but the design would have fewer parts and cost less if a personal computer (PC) is used for all user control. Since the PSoC has a USB port, the receiver can connect to the PC with a USB cable and take power from the PC over the USB cable, saving a power jack, and external power source. Control of the receiver is accomplished by having the receiver USB port appear as a standard com port to the PC. The *Ham Radio Deluxe* (*HRD*) program works perfectly to control this receiver. See Figure 1.

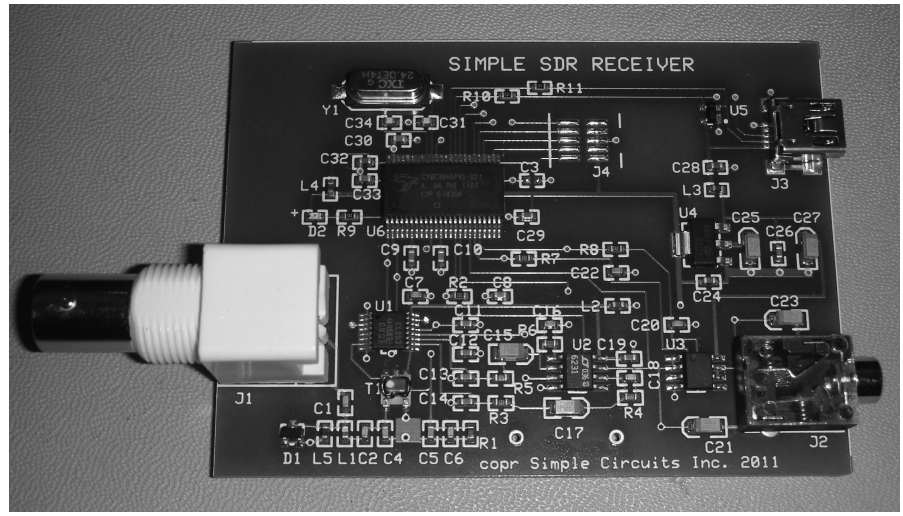


Figure 1 — The complete receiver fits on a 3.2 by 2.3 inch circuit board.

Theory of Operation

This SDR receiver is built using a quadrature sampling detector, as shown in the block diagram of Figure 2. The quadrature sampling detector is nothing more than a set of analog switches that are enabled and disabled in the particular sequence that samples the input signal four times for each cycle of the desired receive frequency. The four samples represent the 0, 90, 180, and 270° points of a sine wave. The detector output is amplified by a pair of op amp low-pass filters. After the op amps, the remaining signal processing is performed inside the PSoC microcomputer using digital processing techniques. The processing will digitize the baseband signal, remove the undesired sideband from the received signal, limit the bandwidth of the audio, and then convert the digital samples back into an analog audio signal.

At the antenna input terminals, an RF low pass filter having a 20 MHz corner frequency suppresses signals above the receiver tuning capability. Figure 3 shows the frequency response for the filter.

Referring to the schematic diagram in Figures 6 and 7, U1, a dual 1-of-4 multiplexer/demultiplexer, is used as the sampling detector. This process is similar in functionality to a local mixer, but the control is performed with digital logic switching levels.

The multiplexer is controlled with two square wave clock signals having the same frequency as the desired receive frequency. The clocks only differ in phase, one being delayed by one-fourth of the clock period. This delay represents the 90° phase shift required for an I/Q type detector.

The PSoC has an internal phase locked loop (PLL) circuit that is used to generate higher clock frequencies from a lower speed clock. The receiver makes use of this circuit to generate the sampling detector clock signals. An external 24 MHz crystal is connected to the PSoC, and is used as the

reference oscillator for the PLL. The PSoC PLL only has the ability to generate frequencies that are integer multiplies of the clock. An additional logic function was created and added to the programmable digital logic section of the PSoC, however, that modulates the PLL divider registers. This effectively turns the PLL into a fractional N frequency synthesizer. The "fractional" term refers to the capability of dividing the PLL feedback signal by a non-integer number, allowing for a frequency resolution as small as desired. For practical purposes, a 14 bit, sigma delta modulator constructed as a 2nd order MASH (Multi-stAge noise SHaping) was written in *Verilog*. This results in a receiver tuning frequency step size of roughly 50 Hz. When a different frequency is selected, the PSoC firmware computes a set of PLL values that will be within 50 Hz from the display frequency.

An external PLL circuit or discrete digital synthesizer chip (DDS) may generate a cleaner clock, but the advantage of using the internal PLL is obviously component cost savings.

The PLL operates in the 56 to 68 MHz range. A divider function added to the programmable digital logic section of the PSoC divides the PLL oscillator down to the desired receive frequency and shifts the phase appropriately between the two output I/Q clocks.

After the mixing process of the sampling detector, a pair of low noise op amps, U2A and U2B, amplify the base band signals. The part was chosen because of its low noise performance and the ability to operate with outputs near the ground and power rails. The op amp inputs are typically in the microvolt range. Since the op amp circuit voltage gain is on the order of 40 dB at 1 kHz, the output signals are on the order of a few hundred microvolts to a few millivolts. This circuit includes a first order low-pass filter having

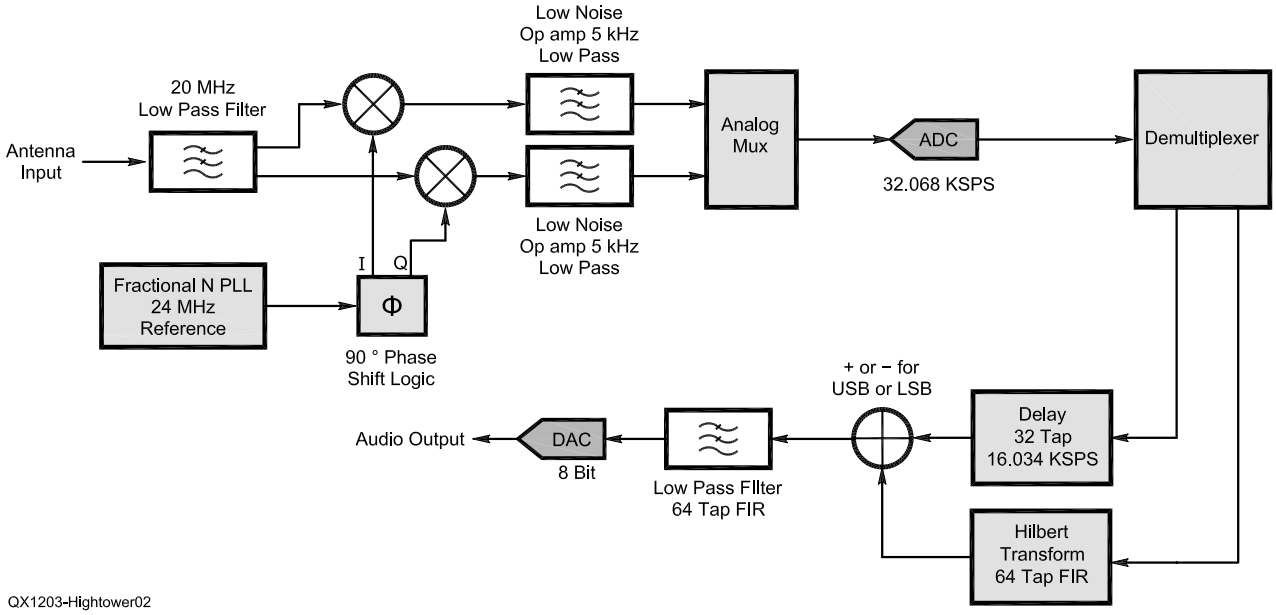


Figure 2 — Here is the Simple SDR receiver block diagram.

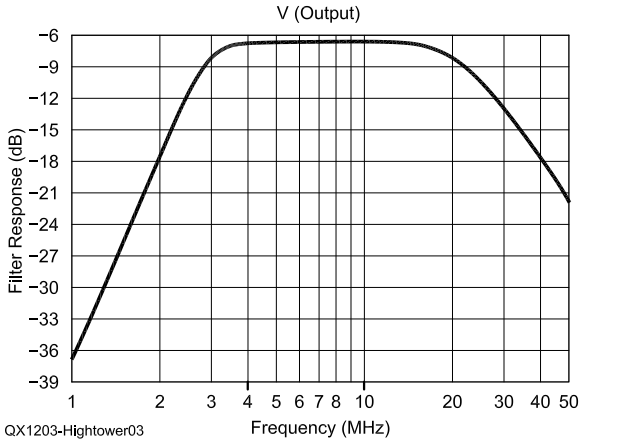


Figure 3 — This graph shows the input RF-filter response.

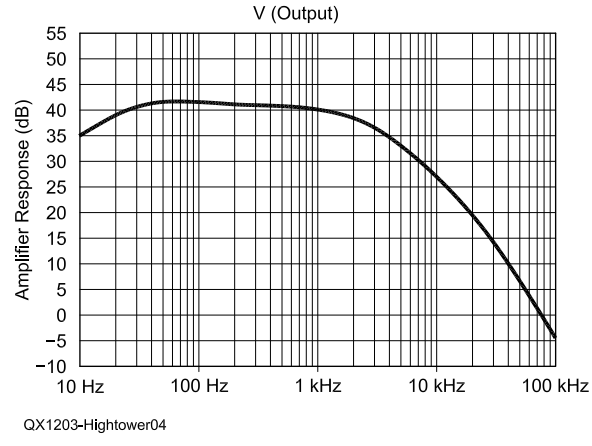


Figure 4 — The op amp circuit frequency response is shown in this graph.

a 3 kHz corner frequency. It is important to reduce the frequencies above half of the analog to digital converter sampling rate, which is called the Nyquist frequency. Otherwise, images will appear at frequencies near the sampling rate. Figure 4 shows the frequency response of the op amp circuit.

From this point, all of the signal processing is performed in the digital domain, and, specifically, inside the PSoC, U6.

The PSoC has a single analog to digital converter (ADC). Since there are two base band signals to process — the I and the Q channels — an analog multiplexer function inside the PSoC is used to switch one of the two inputs to the ADC input. It is desirable to have a high sample rate and a high number of bits, but the best tradeoff found was to use the ADC in a 14 bit mode and sampling at 32,086 samples per second. Since a sample from each input channel is necessary, the equivalent sample rate per channel is 16,043 samples per second. Therefore, the Nyquist frequency is almost 8 kHz. The op amp frequency response at 8 kHz is about 10 dB below the desired passband. This is not great, but leaves room for improvement in a future version.

The PSoC 3 family of parts has an interesting internal hardware feature they call a digital filter block, or DFB, and it consists of a 24 bit fixed point, programmable limited scope DSP engine. This is a dedicated hardware accelerator block that operates independently of the main 8051 processor. It consists of dedicated hardware than can multiply two 24 bit numbers together and add the multiplication result to a 48 bit wide accumulator register, and do this in just one system clock cycle. The process of multiplying and adding is the cornerstone of making signal filters in the digital world. This block is optimized to implement a direct form finite impulse response (FIR) filter that approaches a computation rate of one FIR tap for each clock cycle. This block is used as two independent, 64 tap digital filters.

Alternating outputs from the ADC are loaded into either a 32 sample long-delay line or one of the two digital filters. This digital filter uses a set of coefficients that form an all-pass filter having a flat magnitude response, but phase shifts all frequencies in its passband by 90°. This is called a Hilbert filter. Suppressing either the upper or lower sideband is accomplished by phase shifting the Q channel baseband data and either subtracting or adding the filter output to the delayed I channel baseband data. The delay is necessary to compensate only for the delays incurred by the processing of the Hilbert filter. The output of the addition is one of the two sidebands.

After the removal of the undesired sideband, the data stream is fed into the other half of the PSoC digital filter block configured as a low-pass filter. This filter has a steep roll off as shown in the Figure 5 for a 2 kHz filter. This is the advantage of processing in the digital domain as compared to a set of analog filters. Steep roll offs and repeatability of the filter performance over wide temperature ranges and from part to part variations are the reasons to use digital processing.

The output of the low-pass filter is fed into one of the PSoC's 8 bit digital to analog converters (DAC) that converts the data stream back into an analog signal. This signal is

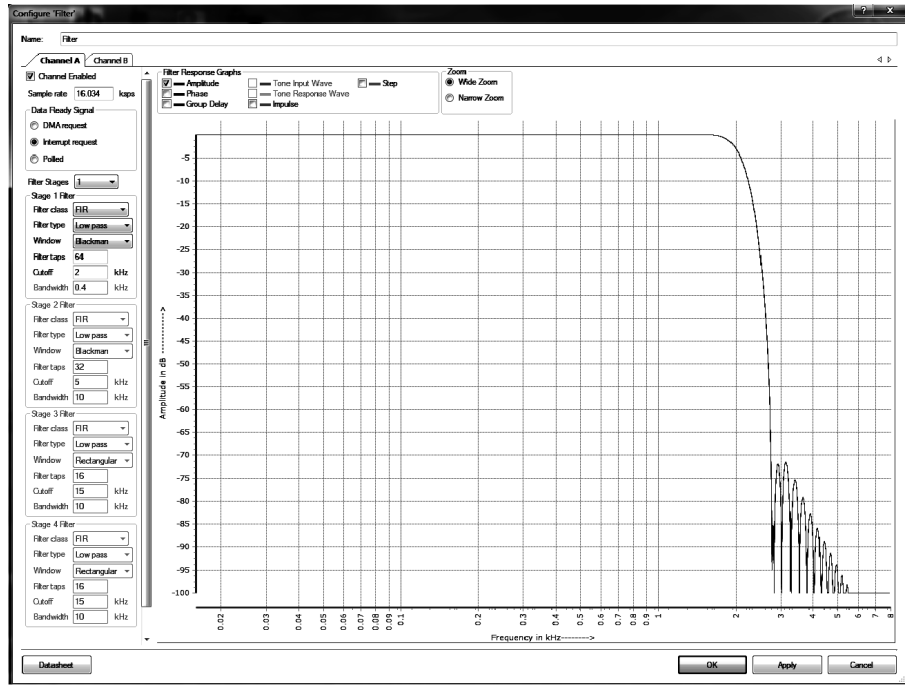


Figure 5 — The 2 kHz audio digital low-pass filter response is shown here.

Figure 6 — The Simple SDR receiver board will fit inside a Hammond Manufacturing model 1455B802 enclosure if a chassis-mount BNC connector is used instead of the on-board connector.

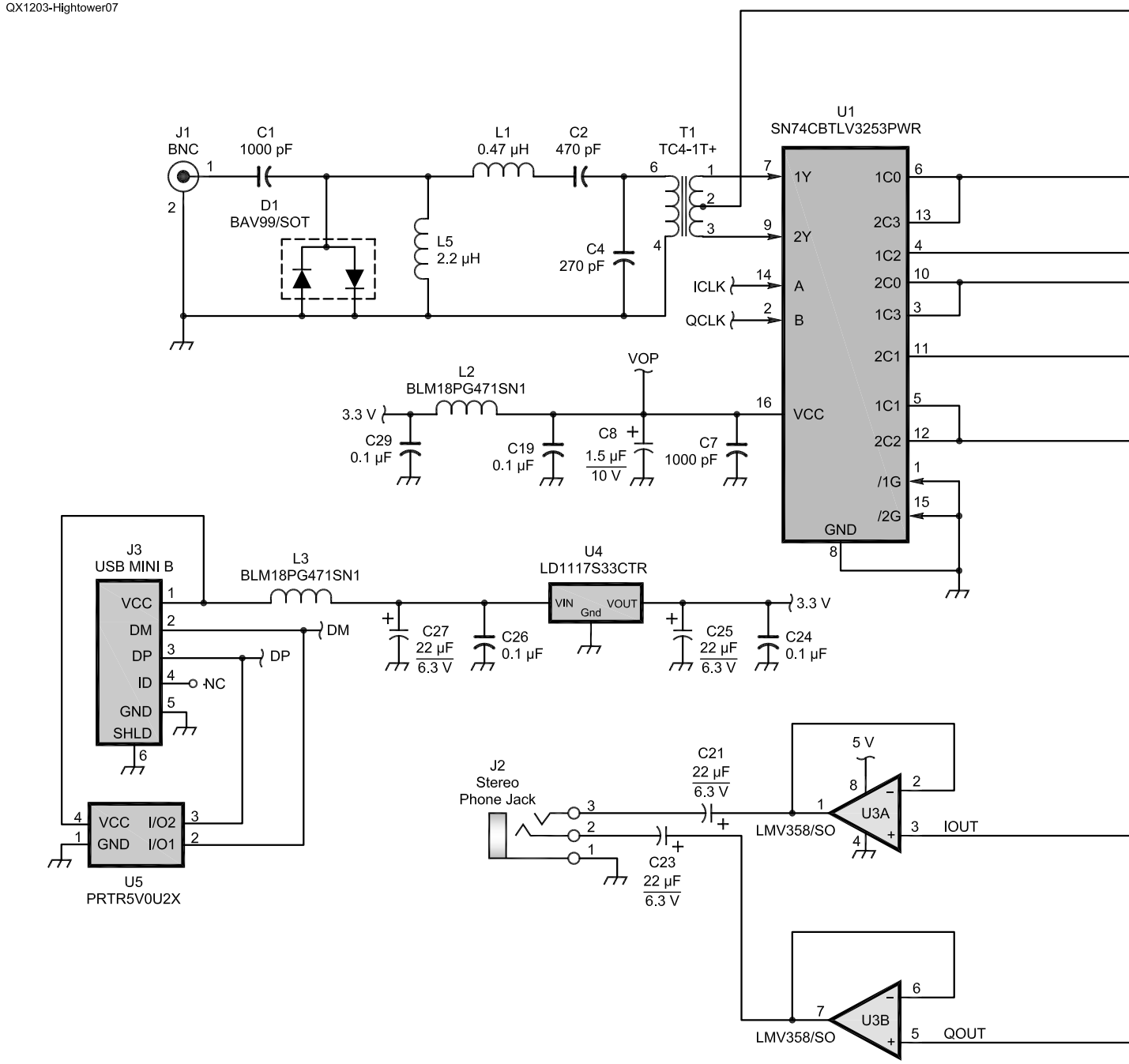
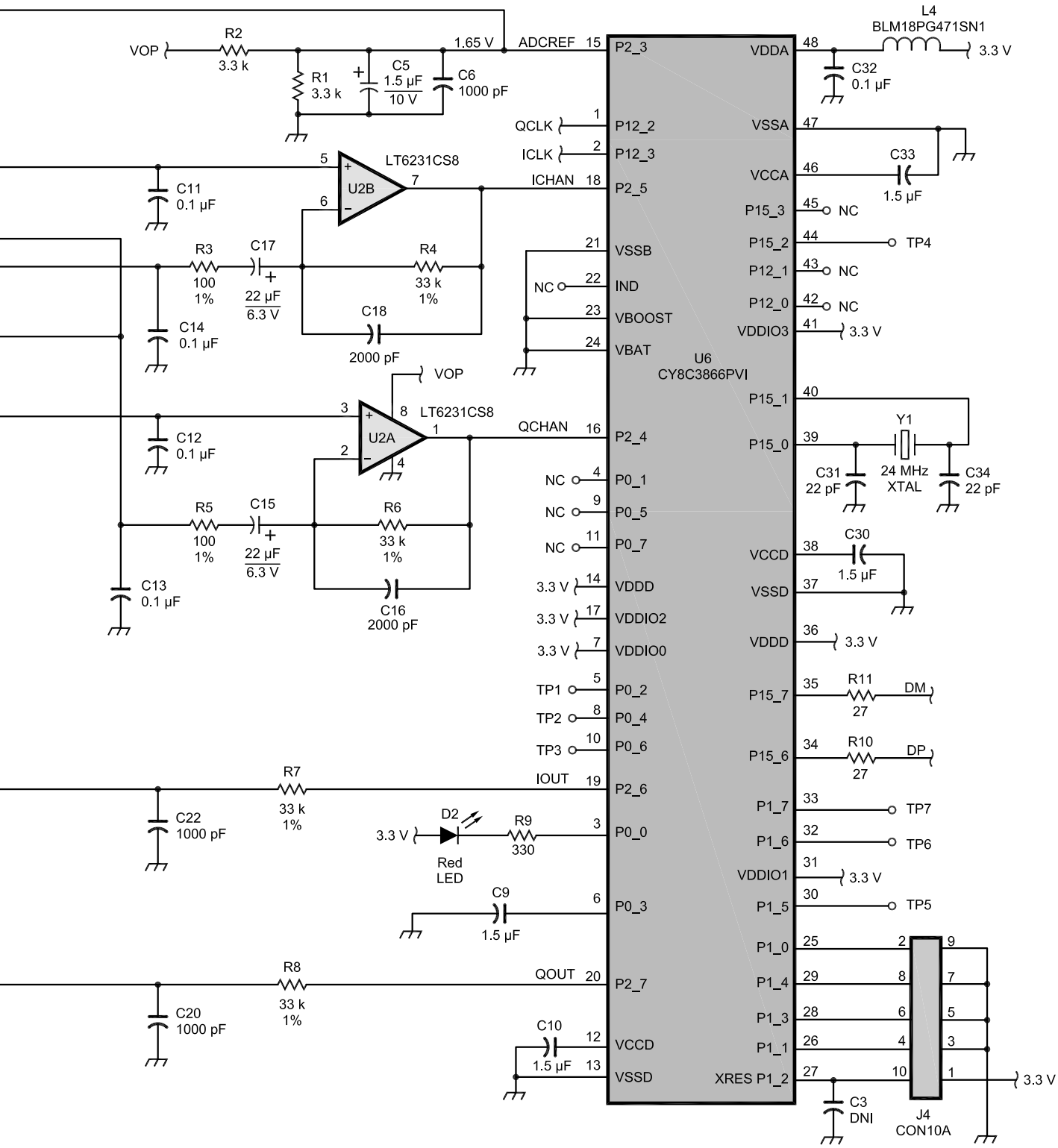


Figure 7 — Here is the schematic diagram of the Simple SDR receiver.


L4
BLM18PG471SN1
3.3 V
VOP
R2
3.3 k
1.65 V
ADCREF 15
R1
3.3 k
C5
1.5 µF
10 V
C6
1000 pF
C32
0.1 µF
QCLK 1
ICLK 2
LT6231CS8
U2B
ICHAN 18
C11
0.1 µF
C33
1.5 µF
VCCA 46
P15_3 45 NC
P15_2 44 TP4
P12_1 43 NC
P12_0 42 NC
VDDIO3 41 3.3 V
R3
100
1%
C17
22 µF
6.3 V
R4
33 k
1%
C18
2000 pF
C14
0.1 µF
NC 22
VSSB 21
IND
VBOOST 23
VBAT 24
U6
CY8C3866PVI
VOP
LT6231CS8
U2A
QCHAN 16
C12
0.1 µF
P15_1 40
Y1
P15_0 39
C31
22 pF
24 MHz
XTAL
C34
22 pF
NC 4 P0_1
NC 9 P0_5
NC 11 P0_7
R5
100
1%
C15
22 µF
6.3 V
R6
33 k
1%
C16
2000 pF
C13
0.1 µF
C30
1.5 µF
VCCD 38
VSSD 37
3.3 V 14 VDDD
3.3 V 17 VDDIO2
3.3 V 7 VDDIO0
VDDD 36 3.3 V
TP1 5 P0_2
TP2 8 P0_4
TP3 10 P0_6
P15_7 35 R11 27 DM
P15_6 34 R10 27 DP
IOUT 19
R7
33 k
1%
C22
1000 pF
P2_6
P1_7 33 TP7
P1_6 32 TP6
VDDIO1 31 3.3 V
P1_5 30 TP5
D2
3.3 V
R9
330
Red
LED
P0_0 3
C9
1.5 µF
P0_3 6
P1_0 25
P1_4 29
P1_3 28
P1_1 26
XRES P1_2 27
R8
33 k
1%
C20
1000 pF
QOUT 20
P2_7
C10
1.5 µF
VCCD 12
VSSD 13
C3
DNI
J4
CON10A
2
9
8
7
6
5
4
3
10
1
3.3 V

buffered with a unity gain op amp, U3, and passed to the output connector.

Modifying and Reprogramming the Receiver

The firmware for the receiver was written and compiled within the Cypress PSoC Creator 2.0 toolset. This toolset contains the graphical design editor used to modify any of the project's internal PSoC hardware modules, the *C* compiler, and it contains tools to reprogram the PSoC flash memory with newly created firmware. This toolset is a free download from the Cypress website. (**www.cypress.com/?id=2494**)

To program a PSoC that has never been programmed, a special programming device that Cypress calls the MiniProg3 is required. Subsequent programming can be performed without using the MiniProg3, however, if the device was programmed with a firmware set that includes a special PSoC bootloader program. Then, further programming can be performed using the USB connection between the PSoC and a computer running the bootloader tool that is included in the PSoC Creator toolset.

I have made the receiver firmware available for download from the ARRL QEX files website.[1] That firmware includes the bootloader program that will communicate with and program the flash memory using the PSoC Creator bootloader tool.

For those who would like to experiment with the hardware, but prefer not to program their own devices and would rather have completed receivers, I will make assembled and programmed receiver boards available. Visit my website at **www.simplecircuits.com** for details.

Performance

The +5 V power to the receiver is supplied by the host USB device, and is typically 55 to 60 mA.

[1]The program files for the Cypress PSoC CY8C3866 microprocessor as well as the *Windows* driver files are available for download from the ARRL *QEX* files website. Go to **www.arrl.org/qexfiles** and look for the file **3x12_Hightower.zip**.

The frequency range of operation is controlled by the firmware. The current firmware limits the tuning to 3.500 MHz to 18.168 MHz. Higher frequencies are beyond the frequency range of the PSoC internal PLL circuit. Lower frequencies, such as the amateur 160 meter band, were overloaded from AM broadcast stations.

The minimum discernible signal (MDS) is approximately –117 dBm.

Installation

Before connecting the USB cable, download the file UARTUSB_CDC.zip and save it on your computer. All of the files associated with this article are available for download from the ARRL *QEX* files website. Unzip the file, put it in any folder, plug in the USB cable, and the computer will prompt you to either let it search for the driver, or allow you to specify the driver location. You will need to specify the location of where you put the file. The receiver has been tested with *Windows XP*, *Vista*, and *Windows 7*.

Note the com port number that your computer assigned to the receiver. Use that com port number in *Ham Radio Deluxe* (*HRD*). In *HRD*, add a new radio, and select Elecraft K2 as the radio type. The speed setting is not important and can be left as the default value.

Operating the Receiver

To operate the receiver, perform the following steps:

1) Connect the USB cable between a computer USB port and the receiver's USB connector, J3. Both power and control are provided by this connection. The PSoC has an internal USB full speed port. The receiver firmware implements a virtual serial communication port. When connected to a personal computer, the receiver will look like a serial com device. Using the standard CDC (communication) drivers that are built into *Windows*, the receiver can communicate with *Ham Radio Deluxe*. The receiver firmware uses the Elecraft K2 communication protocol.

2) Connect an appropriate antenna to the BNC connector, J1. The antenna should support the desired receive frequency.

3) Connect an audio amplifier or headset to the audio output connector, J2, of the receiver. This connector is a stereo connector, but both channels are fed with the same signal. Therefore, the use of either mono or stereo audio devices are acceptable. The receiver audio output will directly drive low impedance headsets. The use of good computer speakers that have a built-in amplifier and volume adjustment is ideal. There is no volume control capability in the receiver. Headsets need their own volume adjustments.

The receiver can be continuously tuned from 3.500 MHz to 18.168 MHz (80 through 17 meters).

Using *Ham Radio Deluxe* to control the radio, the receive frequency, the side band selection, and audio bandwidth can be selected.

There are four different receive filter bandwidth selections. Pressing the *HRD* Filter button produces a drop down menu with various options. FL1 is a 2.5 kHz low pass filter, FL2 is a 2.0 kHz low pass filter, FL3 is a 1.5 kHz low pass filter, and FL4 is a 1.0 kHz band pass filter. FL4 is used for CW and RTTY, and is 400 Hz wide (±200 Hz).

The attenuator button, ATT will decrease the audio volume from strong stations by several dB.

Enclosure

To keep the cost of the receiver as low as possible, the unit is not in any enclosure. The board dimensions were specifically designed to fit in a Hammond Manufacturing model 1455B802 enclosure, however. The on-board BNC connector could be replaced with a through-chassis BNC connector if you want to mount the board in a chassis.

Michael L. Hightower, KF6SJ, has been continuously licensed since 1970, and currently holds an Amateur Extra class license. Active on the HF bands, his interests include homebrew radio design and construction, and experimental communications techniques. Michael earned BSEE and MSEE degrees from the University of Illinois. He is a member of the Institute of Electrical and Electronics Engineers (IEEE), Tucson Amateur Packet Radio Corporation (TAPR) and is an ARRL Life Member.